Area Efficient FPGA Architecture of Arithmetic Cosine Transform Using Vedic Multiplier

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Abstract - Arithmetic cosine transform (ACT) is the optimum algorithm to calculate DCT faster with the utilization of less additions and multiplication operations. This algorithm occupies less area on the chip as well which opens the integration of additional functionality or logic operation on the same chip. Our research work focus on the improvements in the architecture of arithmetic cosine transform (ACT) to achieve improved in terms of area due to future requirements of nano technology. This work proposed an area efficient architecture of the arithmetic cosine transform (ACT) by making updations in the algorithm of addition and multiplication. Here we have used vedic multiplication algorithm to improve the device resource requirement of multiplication operations. The synthesis is performed on the FPGA Virtex 6 chip, and the outcomes show the efficiency of proposed architecture.

Keywords - ACT, DCT, Virtex, FPGA, Vedic Multiplier.

I. INTRODUCTION

The field of computer science is growing at the fastest pace since it started back in the early 20th century. We didn't have the actual computing machines until the mid of the 20th century but the algorithms for computing were already being developed from the beginning of the century. The advancement of the computing field has affected every imaginable field in the human lives.

These fields include engineering, medicine, geology, meteorology, movies, and pictures etc. The high speed of digital computer has contributed to significant progress in the field of optics.

Digital signal processing (DSP) algorithms exhibit an increasing need for the efficient implementation of complex arithmetic operations. The computation of trigonometric functions, coordinate transformations or rotations of complex valued phasors is almost naturally involved with modern DSP algorithms. In this exploration work one of the most computationally high algorithm called the Discrete Cosine Transform is implemented with the help ACT(Arithmetic Cosine Transform) algorithm which results in a multiplier less architectures and comparison is made between the DCT using Chen's algorithm and DCT using CORDIC as well as new CORDIC algorithm.

Discrete cosine transform (DCT) is widely used transform in image processing, especially for compression. Some of the applications of two-dimensional DCT involve still image compression and compression of individual video frames, while multidimensional DCT is mostly used for compression of video streams and volume spaces. Transform is also useful for transferring multidimensional data to DCT frequency domain, where different operations, like spread-spectrum data watermarking, can be performed in easier and more efficient manner. A countless number of research works discussing DCT algorithms is strongly witnessing about its importance and applicability.

Hardware implementations are especially interesting for the realization of highly parallel algorithms that can achieve much higher throughput than software solutions. In addition, special purpose DCT hardware discharges the computational load from the processor and therefore improves the performance of complete multimedia system. The throughput is directly influencing the quality of experience of multimedia content. Another important factor that influences the quality of is the finite register length effect on the accuracy of the forward-inverse transformation process.

Efficient codec circuits capable of both high-speeds of operation and high numerical accuracy are needed for next-generation systems. Such systems may process massive amounts of video feeds, each at high resolution, with minimal noise and distortion while consuming as little energy as possible.

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A class of transforms, called polynomial transforms, has been used heavily for the realization of efficient multidimensional algorithms in digital signal processing. Some of the examples of significant computational savings achieved by using the results from number theory and polynomial transforms include multidimensional discrete Fourier transforms, convolutions and also a discrete cosine transform. The application of polynomial transforms to DCT is not so straightforward as it is the case with discrete Fourier transform and convolutions.

The Arithmetic Cosine Transform (ACT) algorithm consists of only addition and constant multiplication which in turn reduces the computation error. The ACT can be used to calculate the exact and approximate value of the DCT for null mean and non null mean input sequences respectively. The algorithm is with less area complexity and consumes low power.

II. ARITHMETIC COSINE TRANSFORM

The arithmetic cosine transform is a fastest algorithm for DCT calculation of non uniform sample of input signal. the input signal to the DCT is are usually considered as a continuous signal u(t), that are sampled uniformly. this produce a column vector

$$u = \{u_n\}_{n=0}^{N-1} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

Dimension of vector u is N. DCT is represented by the vector u

$$U = \{U_k\}_K^N \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (2)$$

the corresponding non uniform samples of the input sequence u(t) are need to compute the vector U. the instants of sampling are given by

$$S = \frac{2rN}{k} - \frac{1}{2} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (3)$$

where k=1,2,3,N-1 and r=0,1,……k-1

substituting for r=0, k=1 gives s=-1/2

For $r = 1, k = 2$ $s = 15/2$ A set S with sampling points as the elements is defined as

$S = \{All\ values\ of\ S\}$

Let for an 8-point DCT

$$S \in S = \left\{-\frac{1}{2}, \frac{25}{14}, \frac{13}{6}, \frac{27}{10} \dots\dots\dots \frac{15}{2}\right\} \dots\dots\dots\dots (4)$$

To compute DCT ACT algorithm is represented in two ways for non-zero mean sequence and zero mean sequence.

Considering zero-mean sequence, the ACT averages the A_k as

$$A_k = \frac{1}{k}\sum_{r=0}^{k-1} u_{2r\frac{N}{k}-\frac{1}{2}}, k = 1,2, \dots . N-1 \dots\dots . (5)$$

The above expression for ACT from equation (5) averages can be utilized in the computation of DCT of non-uniform input samples.

$$U_k = \sqrt{\frac{N}{2}} \sum_{i=1}^{[\frac{N-1}{k}]} \mu(j).A_{KJ} \dots\dots\dots\dots\dots\dots (6)$$

Where $k = 1, 2 \dots\dots N-1$ and $\mu(j)$ is called mobious function. The ACT is derived by using the Mobius inversion formula. In case of non-null mean input signal, a correction term is subtracted from the equation (6) of to calculate the DCT coefficients and it follows as

$$U_k = \sqrt{\frac{N}{2}} \sum_{i=1}^{[\frac{N-1}{k}]} \mu(j).S_{kj} - \sqrt{\frac{N}{2}}\bar{u}.\ M\left(\left|\frac{N-1}{k}\right|\right) \dots . (7)$$

where $\bar{u}$ is considered as the arithmetic average of the input uniform samples given by

$$\bar{u} = \frac{1}{8} w.v_r \dots\dots\dots\dots\dots\dots\dots\dots\dots (8)$$

with w as the interpolation weight

$$M(n) = \sum_{r=1}^{n} \mu(r) \dots\dots\dots\dots\dots\dots\dots\dots\dots (9)$$

Where M(n) is the Martens function

III. PROPOSED ACT ARCHITECTURE

This work proposed an area efficient architecture of the arithmetic cosine transform (ACT) by making updating in the algorithm of addition and multiplication. A Vedic multiplication algorithm has used to improve the device resource requirement of multiplication operations. Figure 3.1 shows RTL schematic of proposed work top module architecture. The proposed architecture model having 20 ports are v0 to v7 are 16 bit [15:0] width ports and v12, v72, v136, v152, v296, v2514 ,V2710, v5714, v5910, v8914.

The proposed Architecture with sub modules are shown in figure 3.2 there are two vedic multiplier modules are used as demonstrated mul1, mul2, a mean cal module a null mean ACT module 1 and module m3 mertens . The architecture of multiplier is divided into three main categories.

Figure 3.1 RTL View of Proposed Architecture Top Module.

Firstly, the serial multiplier and it is benefit for hardware implementation as it requires only a minimum area of the chip. Secondly, parallel multiplier which is also known as array multiplier and it performs high speed mathematical operations.

Higher consumption of chip area is the main drawback. Lastly, the serial- parallel multiplier and it delivers a satisfactory trade-off between the area consuming. I parallel multipliers and the serial multiplier consuming times. The Vedic multiplier is implemented based on the one of the sutras mathematical formulas that is mentioned in Vedic mathematic literature that is mentioned in the above list. These sutras have been usually used in the decimal number system for the product of two numbers. the similar idea is applied to the binary system in an appropriate way using the digital hardware of the suggested algorithm. Vedic multiplication based on some algorithms such as urdhva tiryakbhyam and nikilam etc.

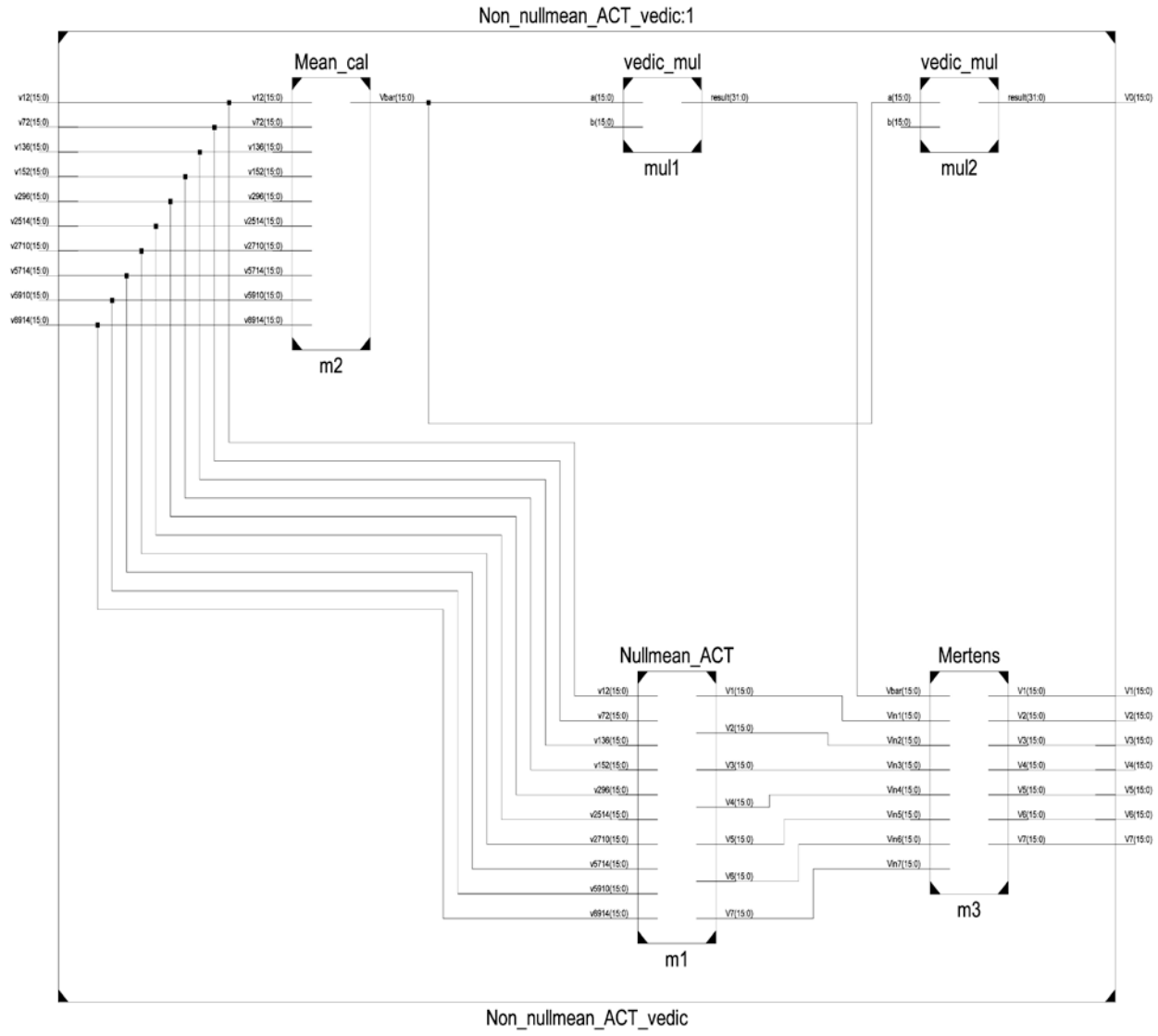

Figure 3.2 RTL View of Proposed Architecture with Sub Modules.

IV. SYNTHESIS OUTCOMES

Implementation and simulation of proposed ACT architecture module has been done on Xilinx ISE performance evaluation and outcome of the proposed work has give in figure 4.1 screen shot of the device utilization summary. Table 1 has given comparative analysis of the proposed work with existing base work.

table 1 has given the result comparison with previous work to proposed work there are two parameters are compared in table 1 which are fixed point word length and another one is no of look up table slice LUTs of FPGA used in for the implementation of proposed work

Table 1: Comparison of Resource Utilization with Previous Architecture

Parameters	Previous Work	Proposed Work
Fixed Point Word Length	8	8
Slice LUTs	756	674

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Device utilization summary:
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Selected Device: 6vlx240tff784-2
Slice Logic Utilization:
 Number of Slice LUTs:                  674  out of  150720     0%
    Number used as Logic:               674  out of  150720     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    674
   Number with an unused Flip Flop:     674  out of     674   100%
   Number with an unused LUT:             0  out of     674     0%
   Number of fully used LUT-FF pairs:     0  out of     674     0%
   Number of unique control sets:         0

IO Utilization:
 Number of IOs:                         288
 Number of bonded IOBs:                 287  out of     400    71%

Specific Feature Utilization:
 Number of DSP48E1s:                     18  out of     768     2%
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Figure 4.1 Device utilization summaries.

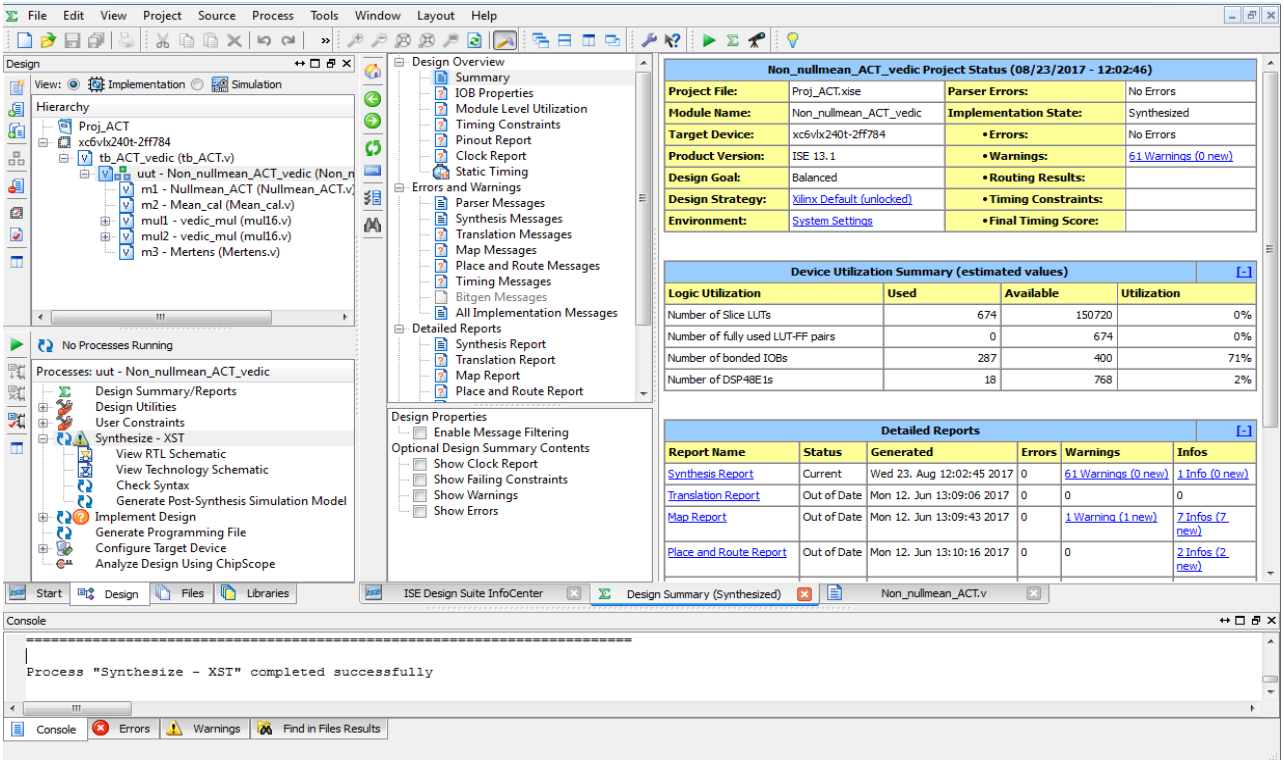

Figure 4.2 Execution Screen Shot of Proposed Architecture.

V. CONCLUSION AND FUTURE WORK

The work present and study various DCT algorithms for the computation of discrete cosine transform and their execution and device utilization. The Discrete Cosine Transform is a champion among the most extensively transfers systems in digital signal processing application mostly for image processing. By considering number of addition multiplications operations needed, computational area complexity and probability of occurrence of error and power consumption, any algorithm can be analyzed for DCT transform. The Arithmetic Cosine Transform is found to be most fast algorithm for DCT computation against most of the popular algorithm. Proposed work has achieved reduced complexity of architecture with only adders and constant integer multipliers which make the structure to be free from the truncation errors occurs with the floating point operations. In this work we have used

two Vedic multiplier instead on constant integer multipliers for fast multiplication operation. Further the proposed algorithm can be utilized for the image processing application using DCT.

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