Compression Techniques - BIST

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Abstract - The conventional testing approach, which involves a bit-by-bit comparison of observed output values with the corrected values as previously computed and saved. This approach requires a significant amount of memory storage for saving the correct outputs associated with all test vectors. In this paper we consider an alternative approach, which is simpler and requires less memory storage. In this approach the information saved is a compressed form of the observed test outcome, called a signature. A circuit is tested by comparing the observed signature with the correct computed signature. The process of reducing the complete output response to a signature is referred to as response compacting or compressing.

Keywords - BIST, One count compression, Transition count compression, Parity check compression and Syndrome test.

I. INTRODUCTION

The importance of delay faults is increasing with newer technologies, and the costs of test pattern generation as well as the volume of test data keep increasing with circuit size, alternative solutions are needed. One such solution is built-in self-test (BIST). The main idea behind a BIST approach is to eliminate the need for the external tester by integrating active test infrastructure onto the chip. Equipping the cores with BIST features is especially preferable if the modules are not easily accessible externally, and it helps to protect intellectual property (IP)[1] as less information about the core has to be disclosed.

There are two widely used BIST schemes: test-per-clock and test-per-scan. The test-per-scan scheme assumes that the design already has existing scan architecture. During the testing phase the TPG fills the scan chains which will apply their contents to the circuit under test (CUT).

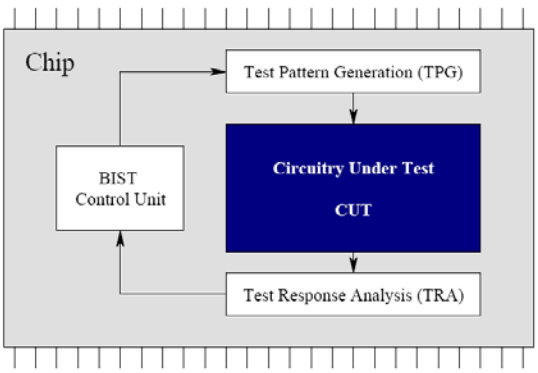

Fig. 1.1 Circuitry under test chip

All scan outputs are connected to the multiple input signature register (MISR), which will perform signature compaction. The test-per-clock scheme uses special registers that perform pattern generation and response evaluation. This approach allows to generate and to apply a new test pattern in each clock cycle. One of the first proposed test-per-clock architectures was the Built-In Logic Block Observer (BILBO), proposed in which is a register that can operate both as a test pattern generator and a signature analyzer.

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As the BIST approach does not require any external test equipment it can be used not only for production test, but also for field and maintenance test, to diagnose faults in field-replaceable units. Since the BIST technique is always implemented on the chip, using the same technology as the CUT, it scales very well with emerging technologies and can become one of the most important test technologies of the future.

II. COMPRESSION TECHNIQUES

We have considered a conventional testing approach, which involves in bit-by-bit compression of observe output values with the corrected values as previously compute and saved. This approach requires a significant amount of memory storage for saving the correct outputs associated with all test vectors, which is simpler and requires less memory storage

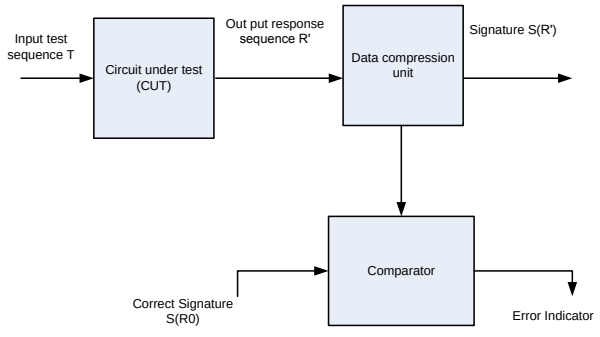


Fig. 1.2 BIST (built in self test) block diagram

The approach the information saved is a compressed the observed test outcomes, called a signature. A circuit is tested by comparing the observed signature with the correct computed signature. The process of reducing the complete output response to a signature is referred to as response compacting or compression.

- Bit-by-bit comparison is inefficient
- Compress information into “signature”.

III. ONE-COUNT COMPRESSION

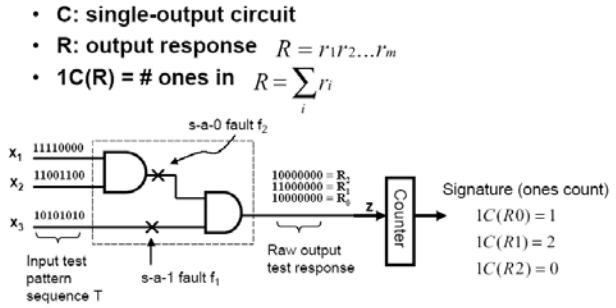


Fig. 3 One count compression by using NAND gate

The number of 1’s in the response stream is calculated and compared to the number of 1’s in the fault –free responses. [3]Consider the circuit shown above, If we have a test of length L and the fault-free count is m, the possibility of aliasing is [C(L,m)-1] patterns out of a total number of possible strings of length L, (2L-1) response compacting or compressing.

IV. TRANSITION-COUNT COMPRESSION

The Transition Count signature is the number of 0-1 and 1-0 transitions in the output response sequence R. Let the response of C to a test sequence be R = r1, r2,.., rm. In transition counting the signature TC(R) is count number of transitions from 0 to 1 and 1 to 0 in a string N bits with i transitions: N-1 boundaries total number of sequences with same TC.

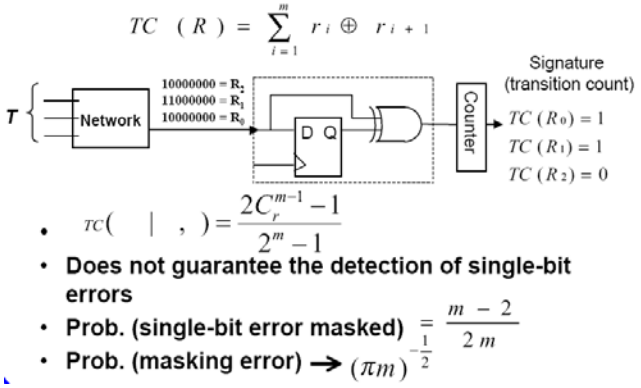


Fig. 4 Tarnsitation count by using gate and flip-flop

V. PARITY-CHECK COMPRESSION

Add parity bit detects all single-bit errors, detects all multiple errors with odd parity masking probability = 1/2 .Multiple parity bits for error detection and correction coding theory:[4] large body of works, especially in communication systems.

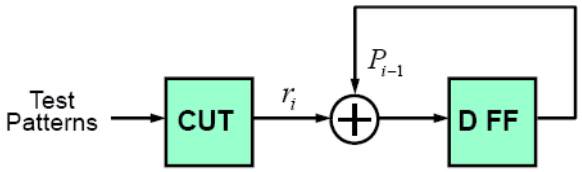
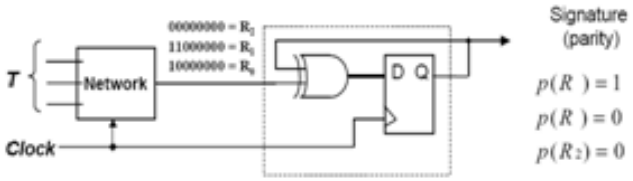


Fig. 5 Parity check compression using D-flip-flop

This is the simplest of all techniques but also the most loss, The parity of responses to the test patterns is calculated as

$$P = \sum_{i=1}^{i=L} r_i$$

where L is the length of the test and *ri* is the response for the *i*th test pattern, The response of the circuit under test (CUT) to pattern *i* and the partial product *Pi-1* .



- Detect all single bit errors.
- All errors consisting of odd number of bit errors are detected.
- All errors consisting of even number of bit errors are masked.
- Probability error masked = $\overline{2}$

VI. SYNDROME TESTING

The syndrome of a Boolean function is $S(f) \equiv \frac{k(f)}{2^n}$, where K is the number of 1s (minterms) *F in* and is the number of independent input variables A typical syndrome testing set-up $0 \leq S(f) \leq 1$ .A circuit is syndrome testable iff fault $S(f) \neq S(f_\alpha)$,

Syndromes of logic gates:

Gate	AND_n	OR_n	XOR_n	NOT
S	$1/2^n$	$1-(1/2^n)$	$1/2$	$1/2$

Table. 1 syndromes of logic gates

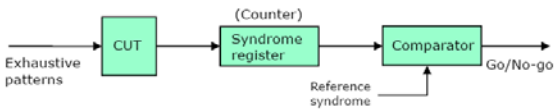
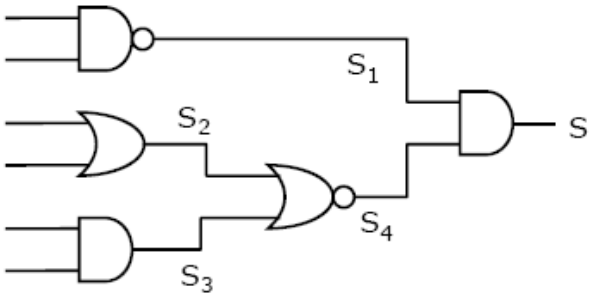


Fig.6 Syndrome circute

Example

Calculate the syndrome of the following circuit



S1 = 1-1/4 = 3/4

S2 = 1-1/4 = 3/4

S3 = 1/8

S4 = 1- S2 - S3 + S2S3 = 7/32

S = S1S4 = 21/128

Consider the function F=XZ+YZ'. The circuit is syndrome untestable If the circuit has a fault, then the corresponding syndrome of the faulty circuit is Thus the circuit is syndrome untestable .A realization C of a function *f* is said to be syndrome-testable if no single stuck-at fault causes the circuit to have the same syndrome as the fault-free circuit. Syndrome is a property of function, not of implementation

VII. SIGNATURE ANALYSIS

Signature analysis is a compression technique based on the concept of cyclic redundancy checking (CRC) and realized in hardware using linear feedback shift registers (LFSR).

A function f(x1,x2,**…**,xn) is said to be linear if it can be expressed in the form of 2n+1 linear functions of n variables.

Linear operations: modulo addition, module scalar multiplication, & delay Nonlinear operations: AND, OR, NAND, NOR, etc

$$f = a_0 \oplus a_1 x_1 \oplus a_2 x_2 \oplus \cdots \oplus a_n x_n$$

where $a_i \in \{0,1\} \forall i = 0,1,\cdots,n$

A linear feedback shift register is a shift register with feedback paths which consist only of unit delays and XOR operators. Let M=fault-free circuit response, B=faulty circuit response, and E=error syndrome (Hamming), where E=MϴB thus M=BϴE and B=MϴE We need a circuit to take B as input and compact it but still be able to tell if M!=B LFSR is considered as a popular approach for test response compaction.

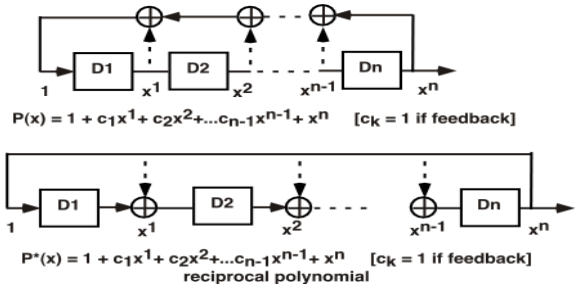


Fig.7.1 Signature analysis is a compression technique based on the concept of cyclic redundancy checking (CRC)

Select P(x) depending on desired fault detection characteristics, primitive polynomial for maximal length, Design LFSR, usually select type 2 to accept external input sequence G(x) via EXOR ,G(x) = Q(x)P*(x) + R(x). Signature = R(x).

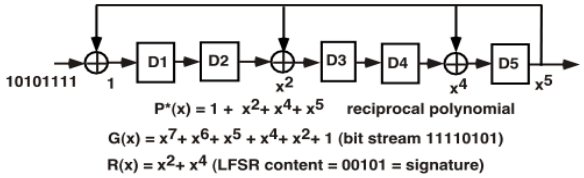


Fig 7.2 linear feedback shift registers (LFSR)

Compression techniques are widely used because their use in self-testing techniques.

All Boolean functions[5] can be implemented by a circuit that is syndrome testable

Signature analysis is the most popular test data compression technique due to low error masking probability

VIII. CONCLUSION

Compression techniques are widely used since they are easy to implement, can be used for field test and self-testing, and can provide high fault coverage, though the correlation between error coverage and fault coverage is hard to predict. BIST is such a test procedure which facilitates testing of circuits before every time they start their operations. In this module we have discussed most of the important components of BIST. A fundamental component in built-in self test. BIST of a system requires techniques for Data Compression, Test Pattern Generation, and Linear Feedback Shift Registers are good for doing both Important concerns Masking Probability, Fault coverage, Overhead Data Compression and Test Generation Functions can be combined in one register.

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