Design and Implementation of Low Power CMOS Lna for Wireless Communication

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Abstract- Thispaper presents the design and implementation of CMOSLNA circuitry. The proposed LNA is designed and analyzed over a frequency of 10-20 GHz range. The design of LNA benefits in great ways like; size, noise figure reduction, gain etc. The simulation result for noise figure and gain are approximately 3 dB and 19 dB respectively. The simulations results obtained have high gain and optimal noise characteristics with good stability. These sorts of LNAs can be utilized in RF receiver for good quality reception. For LNAs, the primary parameters are noise figure and gain. This novel technique may improve the system integration by noise suppression and leading to reduction of chip area and cost eventually.

Keywords- CMOS LNA, Noise Figure, Gain, RF Receiver, System Integration

I. INTRODUCTION

Recently, the trends indicate that there is ever growing emphasis to develop newer devices and innovative design techniques to minimize the power consumption as low as possible. These sorts of technologies improvement have created fresh market segments with a variety of high bandwidth applications and it is also a technology driven perspective. Another perspective is the use requirements based as seen in traditional mobile communication standards such as Global System for Mobile (GSM), Code Division Multiple Access (CDMA) and Wideband Code Division Multiple Access (WDMA) have throughputs of a few megabits per second whereas Ultra-Wide Band (UWB) standard supports data rates of 1 Gb/s [1].

All these are limited to transfer of voice, images and data. The streaming of videos require much higher bandwidths and only communication standards were of capable of supporting the same. The WLAN systems are scalable and can be configured in various topologies to meet the needs of specific applications replacing the need for wired connections i.e. mobile WLAN users can access real-time information at high speed data rates of up to several MG/s downlink. A WLAN operates ubiquitously in the license free bands between 2.4 GHz and 5.8 GHz [2].

Finally, the implementation of a multi-gigabit demodulation employing mixed signal design techniques becomes attractive for the emerging opportunities which requires high speed analog to digital converter (ADC) with low resolution. The high speed ADC and broadband demodulation for wireless systems too offers many advantages over traditional analog demodulation. Eventually, the merits of a high performance mixed signal receiver such as sensitivity, data rate, signal dynamic range, bit error rate and power are directly related to the quality of the embedded ADCs.The high speed signal processing and data converters are incorporated in almost all modern multi-gigabit communication systems [3].

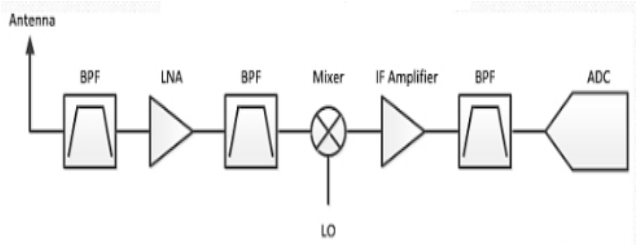

Figure 1: A block diagram of a RF Receiver

II. CMOS PROCESS TECHNOLOGY

Two important characteristics ofcomplementary metal oxide semiconductor (CMOS) devices are high noise immunity and low static power consumption. Since, one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic i.e., Transistor-Transistor Logic (TTL) of NMOS logic which normally have standing current even when not changing state. The CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI based chips [4].

With the rapid progress in semiconductor technology, chip density and operation frequency have increased, making the power consumption in battery operated portable devices a major concern. High power consumption reduces the battery service life. The goal of low power design for battery powered devices is thus to extend the battery services life while meeting performance requirements. Basically, the reducing power dissipation results in increased packaging and cooling costs as well as potential reliability problems. Probable electronic devices

tend to be much more complex than a single VLSI chip. They contain many components ranging from digital and analog to electro-mechanical. The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in integrated circuit technologies and very large scale CMOS design [5].

Much of the power dissipation in portable electronic devices comes from non-digital components. Dynamic power management which refers to a service, shut-off or slowdown of system components that are idle has proven to be a particularly effective technique for reducing power dissipation in such systems. Incorporating a dynamic power management scheme in the design of an already complex system is a difficult process that may require many design iterations and careful debugging and validation. Regardless of application, the use of aggressive voltage scaling can lead to considerable energy reductions whenever performance demands are low for a circuit [6].

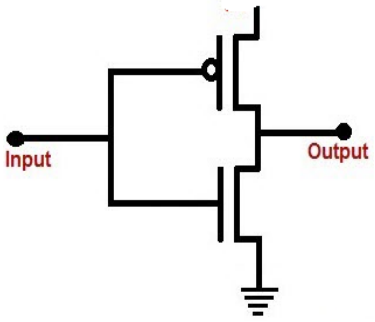

Figure 2: CMOS inverter circuit

The characteristic equations that will be used to model an n-channel MOSFET are as follows:

I. CUT-OFF Region:

$$V_{GS} < V_T$$

$$I_D = 0$$

II. TRIODE Region:

$$V_{GS} > V_T$$

$$V_{DS} < V_{GS}-V_T$$

$$I_D = K(2 (V_{GS}-V_T) VD_S -V_{DS2})$$

III. PINCH-OFF Region:

$$V_{GS} > V_T$$

$$V_{DS} > V_{GS}-V_T$$

$$I_D = K (V_{GS}-V_T)2$$

A p-channel MOSFET works the same as the n-channel except that it has negative voltages and currents. The equations are the same except that the subscripts are reversed for the relative voltages. Thus, in the three regions

I. CUT-OFF Region:

$$V_{GS} < V_T$$

$$I_D = 0$$

II. TRIODE Region:

$$V_{GS} > V_T$$

$$V_{DS} < V_{GS}-V_T$$

$$I_D = - K(2 (V_{GS}-V_T) V_{DS} -V_{DS2})$$

III. PINCH-OFF Region:

$$V_{GS} > V_T$$

$$V_{DS} > V_{GS}-V_T$$

$$I_D = - K (V_{GS}-V_T)2$$

For this convention, V_T still must be used as the absolute value or a positive number. Also, as noted by the negative sign, the current is leaving the drain rather than entering the drain as in the n-channel [7].

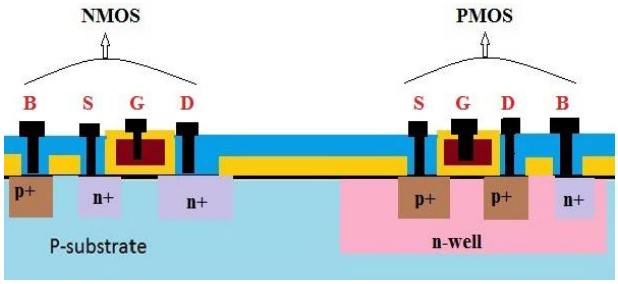

Figure 3: CMOS schematic diagram

III. PROPOSED LNA SYSTEM ARCHITECTURE

Low noise amplifiers (LNAs) are generally used in many systems where low level signals must be sensed and amplified accordingly. LNAs are typically used in communication transceivers for the amplification of the weal electrical signals. Importantly, an LNA is capable of decreasing most of the incoming noise and amplifying a desired signal within a certain frequency range to increase the signal to noise ratio (SNR) of the communication system and improve the quality of received signal as well. An LNA is basically utilized in various aspects of wireless communications including cellular network communication, Local Area Networks (LANs) and satellite communications. A critical building block in a radio receiver is the LNA [8].

An LNA is used in conjunction with numerous frequency functions e.g., mixers, voltage controlled oscillators (VCOs), limiters, filters etc. A typical receiver foe a radio frequency signal comprises a combination of an amplifier and a mixer for signal amplification and frequency conversion. The amplifier generally an LNA receives a combination of an amplifier and a mixer for signal amplification and frequency conversion. The amplifier

usually an LNA receives the Radio Signal(RF) signal amplifies the RF signal and feeds the amplified RF signal to the mixer which in addition receives a local signal from a local oscillator (LO). The LO signal has a frequency which is different from the frequency of the RF signal. The mixers generate an output signal that includes more frequencies than the frequencies of the RF signal and the local signal. The output signal is usually filtered to block undesired frequencies which include the original frequencies, their harmonics and their sum frequencies [9].

The LNA amplifies the received signal and boosts its power above the noise level produced by subsequent circuits. The performance of the LNA greatly affects the sensitivity of the radio receiver. In a receiver, the RF signal is received by an antenna then amplified using a fixed gain amplifier and transmitted over a transmission line having characteristic impedance to the receiver circuitry. Since, the received RF signal strength can vary significantly depending on the distance between the receiver and the transmitter; RF receivers typically include a circuit for automatic gain control (AGC). The signal at the other end of the transmission line is then typically amplified in a variable gain LNA whose gain is controlled by the AGC circuit before being converted from RF to baseband.Using an LNA, the effect of noise from subsequent stages of the receiver chain is reduced by the gain of the LNA itself is directly into the received signal. Therefore, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible so that the retrieval of this signal is possible in the latter stages in the system. [10].

IV. RESULTS & ANALYSIS

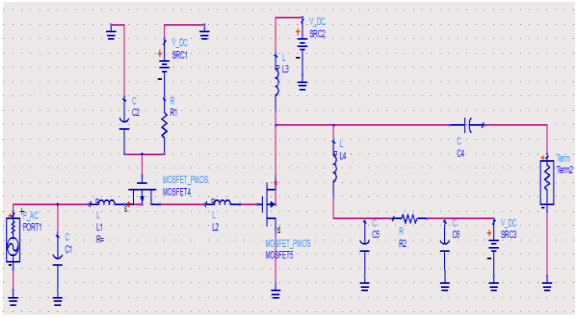

Figure 4: The schematic of the proposed LNA

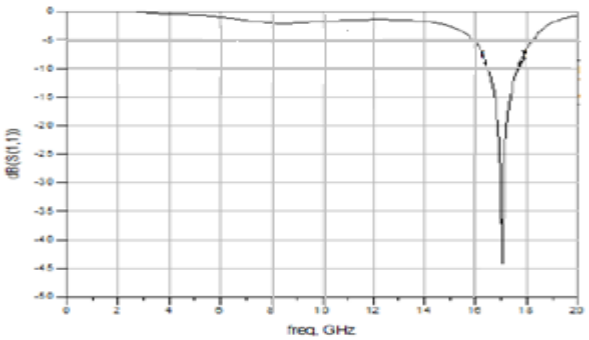

Figure 5: Input Match ImpedanceVs. Frequency

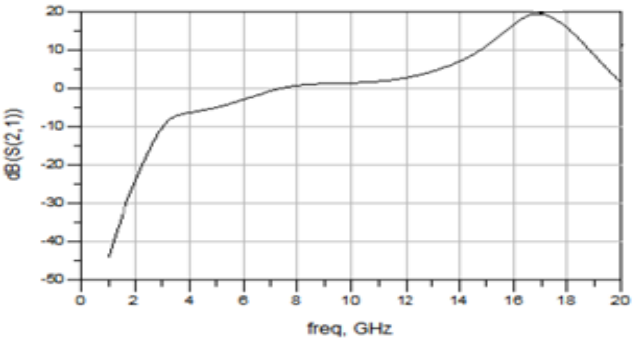

Figure 6: Gain Vs. Frequency

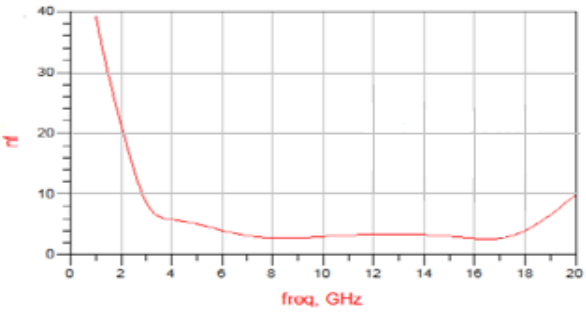

Figure 7: Noise Vs .Frequency

V. CONCLUSION

The integration of CMOS LNA with the circuit system remains to be a daunting challenge for wireless communication.The CMOS LNA improves performance parameters at high frequency and achieves low noise figure and high gain of approximately 3 dB and 19 dB respectively. Noise is an important parameter which has a direct impact on the cost, performance and required design time for wireless receivers. The measurement of noise figure in low noise elements has become particularly important to the development of next-generation communication systems. It has necessitated the needfor the process of making feasible noise figure measurement of LNA. In the future, significantly power consumption can be saved by further exploring the performance trade-offs in wideband applications.

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