Development of Low Power SOLS Based Encoding Architecture for DSRC Applications

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Abstract - The vehicular ad hoc network (VANET) is a kind of wireless ad hoc network which deploys the concept of continuous varying vehicular motion. Here, the moving vehicles act as nodes. It is an active area research right now and emerging type of network aimed at improving safe driving, traffic optimization and some other services through vehicle to infrastructure communication (V2I) or vehicle to vehicle communication (V2V). In this work the work pointing towards the consumption of power and speed of the system to generated FM0 or Manchester encoding using SOLS technique. Here the SOLS is modified to increase the system calculation speed and to reduce the consumption of power. The power consumption is 15mW and frequency of the system is 358.111 MHz.

Keywords - Modified SOLS, Frequency, Speed, Power Consumption, DSRC Application.

I. INTRODUCTION

Dedicated Short-Range Communications (DSRC) is a promising wireless innovation which works in the range of 5.9 GHz with spectrum of 75 MHz It is a wireless protocol standard still being worked on which is intended to support vehicle-to-vehicle and vehicle-to-system communication. Its basic role is to bolster basic safety applications which will decrease the number of road accident and as a result about and subsequently will diminish the number of life lost and second purpose is to enhance traffic flow, although beside these two, private services will also be allowed. DSRC will have six service channels and one control channel .The control channel will be utilized for the transmission and reception of “life safety" messages and furthermore service promotions and the service channels will be utilized for other non-security basic messages.

Engineers are regularly stood up to enhance the system usefulness and exhibitions objective while at the same time augmenting the battery life of electronic devices. From the consumer’s perspective, they are expecting increasingly functionality in small devices that works for quite a while, whose battery does not should be changed regularly. The regular point is the battery; the upkeep cost can be high and sometimes the substitution is truly troublesome (e.g.: sensors inside the dividers of a house). To successfully outline electronic devices with a more extended battery life, or even without battery, one ought to consider the power streamlining at all levels, from the circuit engineering up to the application layer. These days, Wireless Sensors (WS) can understand three exercises, with the related energy cost, Fig.1.1.

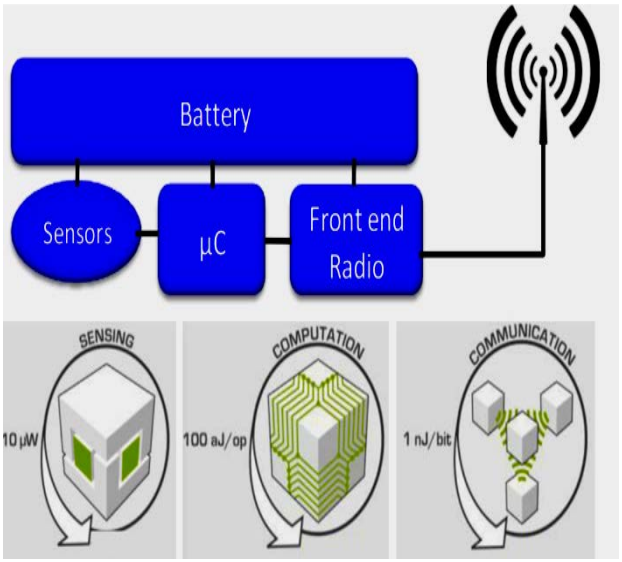

Figure 1.1 Classical WS diagram illustrating the different power consumption for each operation mode.

II. SYSTEM MODEL

A. VANET

Vehicular Ad Hoc Network (VANET), and the RSUs are additionally associated with the spine network by means of the fast network associations. An expanding interest has been raised as of late on the applications through V2V and V2I communications, planning to enhance driving safety and traffic management while furnishing drivers and travelers with Internet get to. It is evaluated that the market for vehicular communications will reach to multi-billion dollars by 2012.

In VANETs, RSUs can give help with finding the offices, for example, eateries and corner stores, and broadcast traffic-related messages, for example, "most extreme bend turning speed" notices to surrender drivers a heads. For instance, a vehicle can convey to a traffic light through V2I communications, and traffic light can demonstrate to

the vehicle when swinging to yellow or red. This can be filled in as guidance ahead of time sign to the drivers, and will be extremely useful to the drivers when they are driving amid winter climate conditions or in a new region, particularly when confronting a wide point of road bend in front of a traffic light. This could decrease the event of red light running with a calamity condition. Through V2V communications, then again, the drivers can show signs of improvement consciousness of what's happening in their driving condition. Figure 2.1 demonstrate model of Vehicular ad hoc networks.

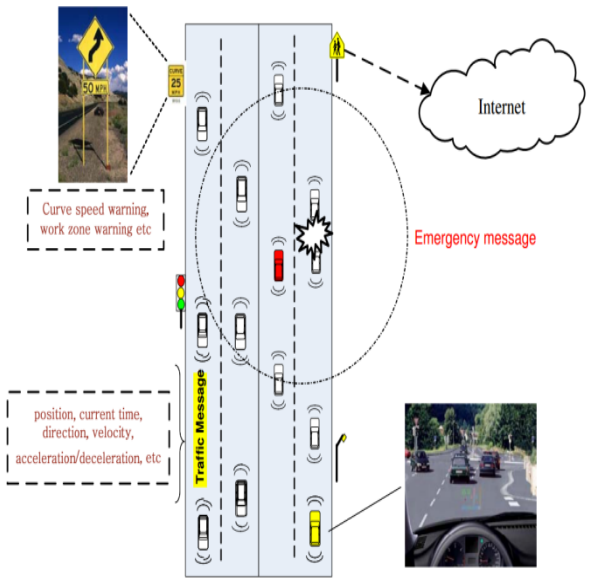

Figure 2.1 Vehicular ad hoc networks.

B. DSRC Protocol Overview

Dedicated Short-Range Communications Protocol is a multi-channel wireless protocol, still being worked on, that depends on the IEEE 802.11a Physical Layer and the IEEE 802.11 MAC Layer. It works over a 75 MHz authorized spectrum in the 5.9 GHz band assigned by the FCC for the support of low inactivity vehicle-to-vehicle and vehicle-to-framework communications.

The motivation behind the development of DSRC is based mainly on the need for a more tightly controlled spectrum for maximized reliability. The utilization of hand-held and hand free devices that possess the 2.4 and 5 GHz bands alongside the expansion of WiFi could bring about intolerable and uncontrollable levels of interference that would essentially diminish the unwavering quality and adequacy of vehicular safety applications. Yet, even with an authorized band, a few issues emerge, for example, reasonable access to all applications, including need planning of movement between various application classes (safety over non-safety).Unlike 802.11, multi-channel coordination is a basic capacity of DSRC. DSRC is like 802.11a, yet there are still some real contrasts:

Operating Frequency Band: DSRC operates in a dedicated 75 MHz spectrum in a 5.9 GHz band, but IEEE 802.11a operates only on the unlicensed portions of the 5 GHz band.

- Application Environment:

DSRC should work in an outdoor high - speed condition rather than 802.11a which is intended for indoor WLAN. This brings new issues for wireless channel proliferation considering the multi-way postponement and Doppler impacts brought about by fast.

MAC Layer: The DSRC band is isolated into 7 channels, one control channel to bolster safety applications and 6 service channels to bolster non-safety applications. Organizing safety messages over non-safety ones is one of the DSRC MAC layer capacities, this being identified with multi-channel coordination. Beside this, the MAC layer takes after the first 802.11 MAC.

- B. Physical Layer:

The bandwidth of each DSRC channel is 10 MHz, rather than 20 MHz divert in 802.11a. This directly affects the greatest information rate it can bolster (27 Mbps) , and timing parameters and recurrence parameters. Likewise the transmit control cutoff is unique in relation to that of the 802.11a protocol. Beside these distinctions, it takes after a similar casing structure, 64-sub-carrier OFDM based modulation conspires.

III. PROPOSED ARCHITECTURE

To enhance the signal reliability in communication system the signal needs to be encoded before transmission. But FM0 and Manchester encoding reduces the performance of the VLSI architecture to maintain diversity in encoding. To overcome this problem the architecture is optimized using SOLS technique in the previous researches, and now further optimizing in this paper using modified SOLS technique. The modified architecture of the system significantly reduces the power utilization and speed up the calculation as circuit works on higher frequency.

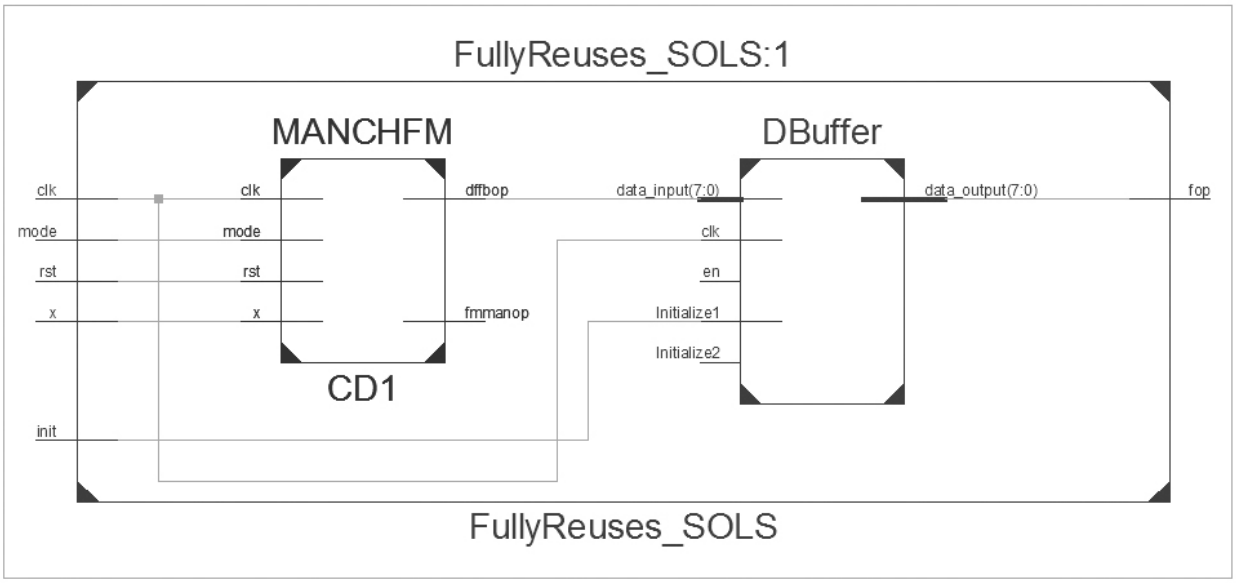

Figure 3.1 Top Module of Proposed Architecture (SOLS FM/Manchester and Delay Buffer)

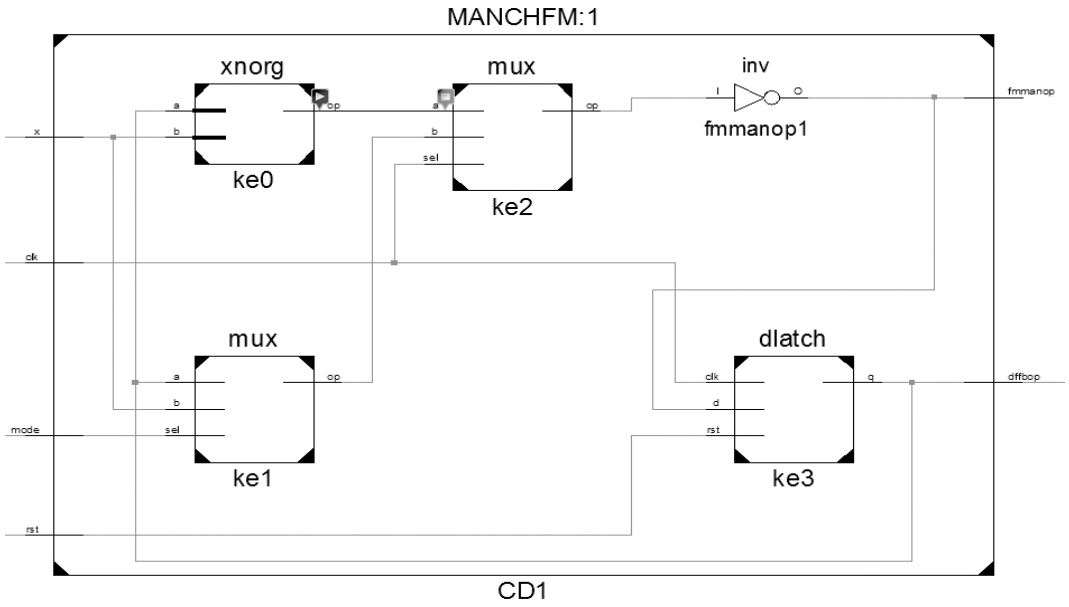

Figure 3.2 SOLS FM0 Manchester Block

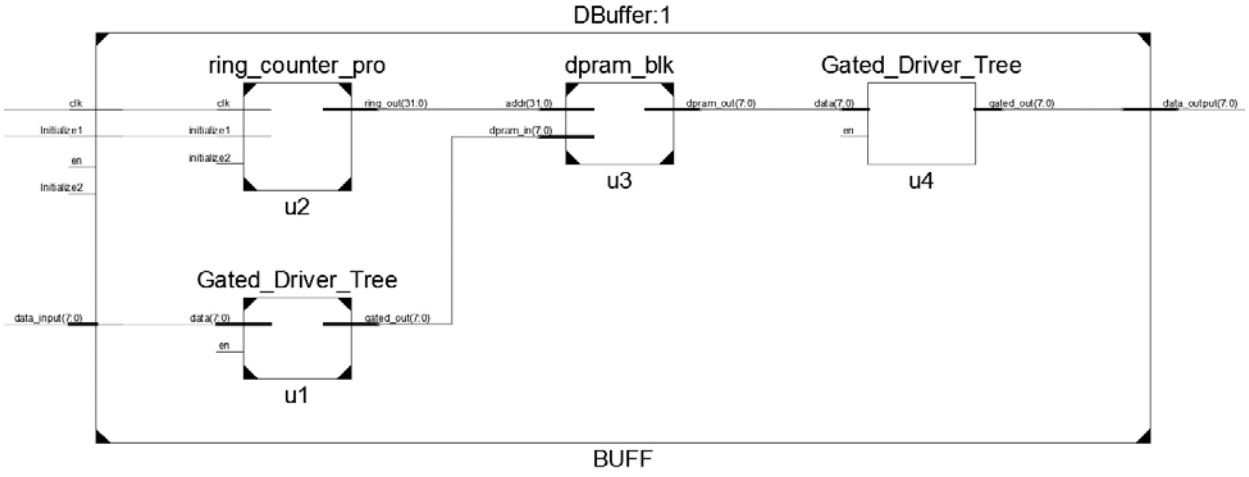

Figure 3.3 Delay Buffer Modules

IV. SYNTHESIS OUTCOMES

The proposed system has designed implemented and synthesized on Xilinx ISE design suit XILINX User Interface of proposed system architecture showing device utilization summary has demonstrated in Figure 4.1. Devise utilization summary of the proposed system has illustrated in Figure 4.2 frequency of the proposed system is 358.11 MHz on clock period 2.79 ns.

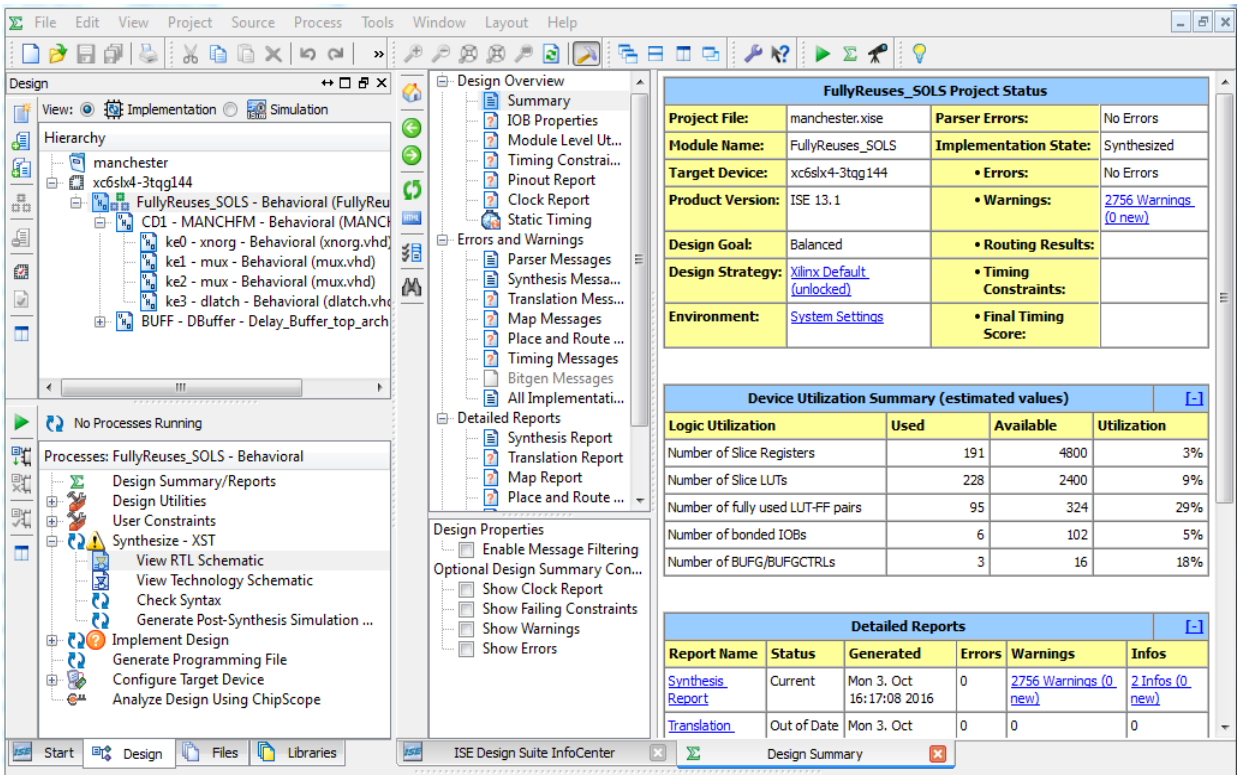

Figure 4.1. XILINX User Interface of proposed system architecture showing device utilization summary.

Table 1 illustrated the comparison parameter of proposed system with existing system. With the following parameter consideration device utilization, power consumption, frequency.

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Timing Details:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.792ns (frequency: 358.111MHz)
  Total number of paths / destination ports: 1 / 1
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Figure 4.2. Frequency of the proposed architecture 358.111 MHz

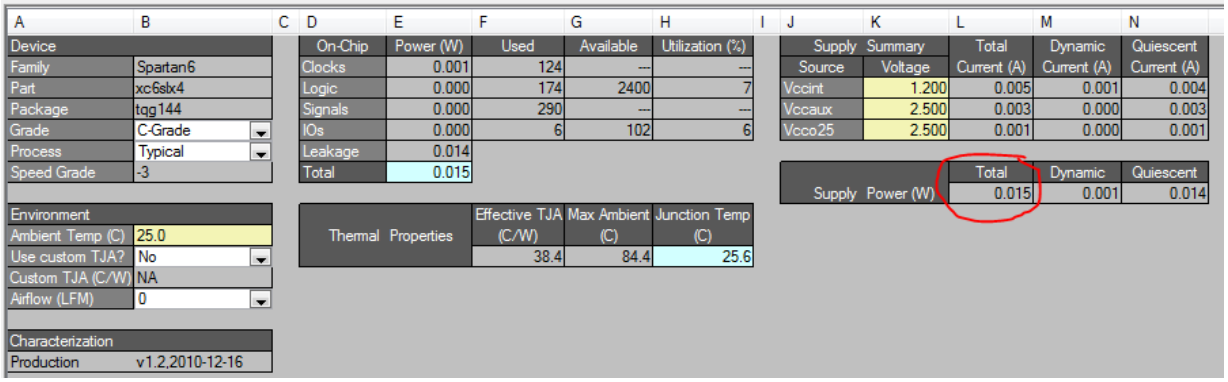

Figure 4.3 Power Consumption of Proposed Architecture 27mW

Table 1: Comparison of Parameters

System	Device Utilization	Power Consumption	Frequency
Proposed System	Spartan 6	15 mW	358.111 MHz
Existing System	Spartan 2	28.30 mW	296 MHz
Improvements		46.99%	21.84%

V. Conclusion and Future Scope

The proposed system is analyzed and synthesized in the XILINX which shows different outcomes of the architecture tested. The proposed architecture is optimized to speed up the system and consume less power than the previous system. The frequency and power consumption is better than the previous system which is explained in the Table 1 in previous section of the paper. Here the proposed system has 46.99% improvements and 21.84% improvements in frequency and power respectively. The upcoming or further work can be focused on to improve the nano meter architecture of FPGA to implement same design as well as in the front end design we can design system for higher number of bit processing with modifications in buffer and encoding technologies.

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