Minimizing Offset in Sense Amplifier using AFGA

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Abstract: This paper deals with offset correction techniques for voltage sense amplifiers using self adaptive circuit that is autozeroing floating gate amplifier. Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories. Their performance strongly affects both memory access time, and overall memory power dissipation.

I. INTRODUCTION

An amplifier is an electronics circuit used in electronics device to increase voltage, current, or power of the signal. Amplifiers are used in wireless communication, broadcasting, audio equipment, medical equipments, biomorphic circuit etc. Amplifiers are commonly used circuit in electronics to increase the amplitude of signal waveform without changing other parameters. Amplifier is one of important circuit in electronics equipment because it takes a very weak signal as input and amplify that signal to give proper output, for example in biomorphic circuit a very weak signal generated nerves or tissue must be amplify so that it is sense by any other sensor. Important parameter which effect the performance of an amplifier and hence the performance of overall system is amplifier noise. Noise is the unwanted signal in any desired signal which degrades its performance. Noise may be generated in an amplifier due to many reasons. Some of the low frequency error which generally affects the amplifier performance are offset, 1/f noise and drift. Offset is caused due to manufacturing variation in MOS technology. 1/f noise is result of defect in interface between gate oxide and substrate. Previously several works are done to reduce noise in amplifier. For designing high precision circuit, it is necessary to reduce the offset, one of the alternative for this is to use component with low offset. Therefore auto-zeroing technique came into existence which is used to reduce the offset in the input of the amplifier. Auto Zeroing Amplifier uses a nulling amplifier for offset correction. But using a operational amplifier for auto-zeroing may increase the chip area therefore its better to use CMOS based auto zeroing technique. In amplifier design in CMOS technology which includes auto zeroing technique for voltage offset. This amplifier may be suitable for low DC signal instrumentation.

Using a conventional auto zeroing amplifier require a more number of transistor because a complete operational amplifier is used. Therefore Autozeroing floating gate technique may be used. Autozeroing floating gate amplier circuit is the first to use hot electron enjection. It reduces its offset as the natural part of its operation.

II. AFGA DESIGN

Implementation

An autozeroing floating gate amplifier circuit consist of two transistor pMOS and nMOS as in figure 1. Gate of pMOS is connected with capacitor C1which work as a floating gate and C2 is connected as feedback between gate and drain of pMOS. Floating gate of pMOS is connected to Vtun. Input Vin will be given at capacitor C1.An AFGA work on the principle of tunneling and hot electron injection.

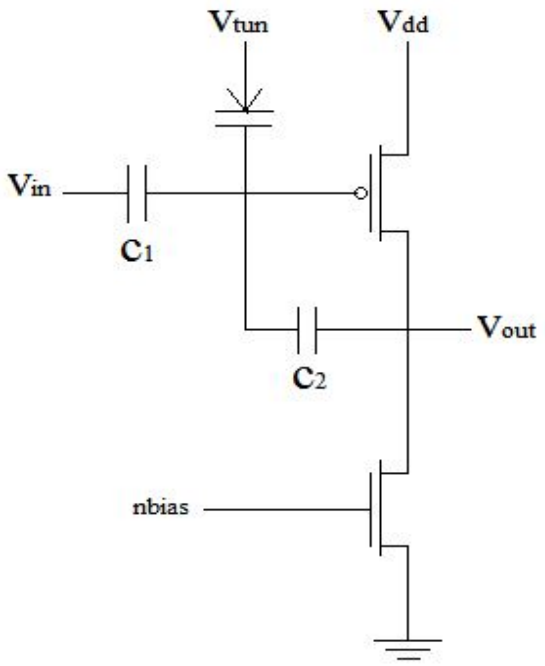

Figure: 1 Circuit of the autozeroing amplifier using the hot-electron injecting pMOS. The ratio of C2 to C1 sets the gain of this inverting amplifier. The nMOS is a current source and sets the current through the pMOS. Steady state occurs when the injection current equals the tunneling current.

Because of feedback capacitor input signal is amplified by close loop gain, which is approximately equal to –C1/C2. Output of the AFGA is stabilize by combination of tunnelling and hot electron injection. The output is stabilize

by increasing the power supply and Vtun. When Vtun is increase more charge are store on the floating gate which increase threshold voltage of pMOS, which drop the steady state output voltage. Increasing power supply voltage, increase the drain to source voltage, which increase the injection current. Increasing power supply decrease tunnelling current and decrease steady state output voltage. During injection source and drain are at high voltage because of this some of the charge get trap in the floating from the channel, which decrease the threshold voltage of pMOS. With combination of this hot electron injection and tunnelling autozeroing floating amplifier reduce any noise in the input signal as a natural part of its operation.

Simulation result

We have simulated AFGA circuit using HSPICE. We consider step in input signal as a noise and check how AFGA reduce this noise

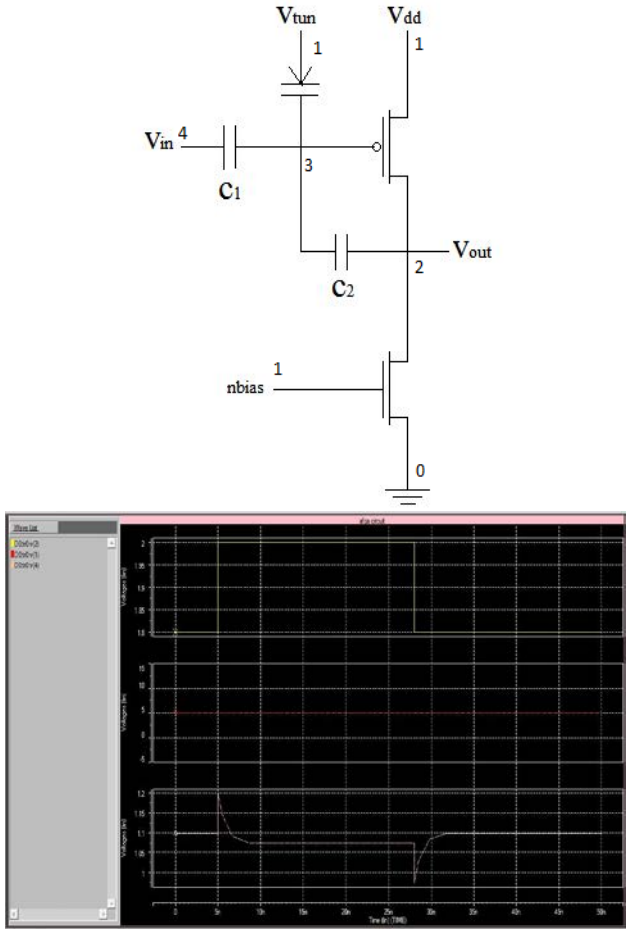

Figure: Simulation of AFGA on hspice

III. USE OF AFGA IN SENSE AMPLIFIER

Sense Amplifier is the most vital circuits in the periphery of CMOS memory as its function is to sense or detect stored data from read selected memory. The performance of sense amplifiers strongly affects both memory access time and overall memory power dissipation. The fallouts of increased memory capacity are increased bit line capacitance which in turn makes memory slower and more energy hungry. In modern computer memory, a sense amplifier is one of the elements which make up the circuitry on a semiconductor memory chip (integrated circuit); the term itself dates back to the era of magnetic core memory. A sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bitline that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory.

Modern sense-amplifier circuits consist of two to six (usually four) transistors, while early sense amplifiers for core memory sometimes contained as many as 13 transistors.[3] There is one sense amplifier for each column of memory cells, so there are usually hundreds or thousands of identical sense amplifiers on a modern memory chip. As such, sense amplifiers are one of the only analog circuits in a computer's memory subsystem.

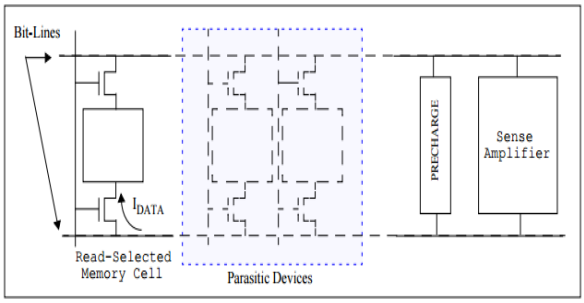

Figure: Sense amplifier with memory cell

IV. APPLICATION OF AFGA IN SENSE AMPLIFIER

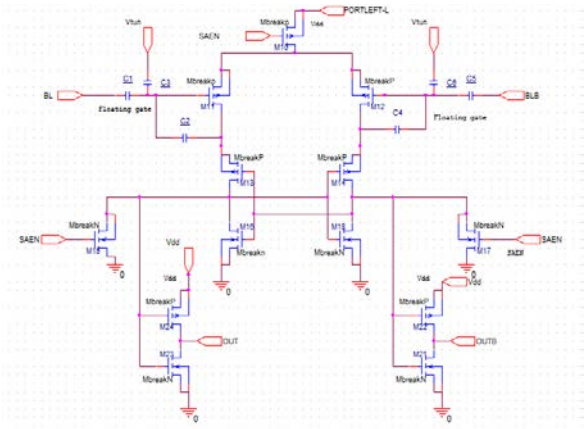

Figure. A schematic diagram of a Sense amplifier with AFGA at the input(BL and BLB)

V. SIMULATION RESULT

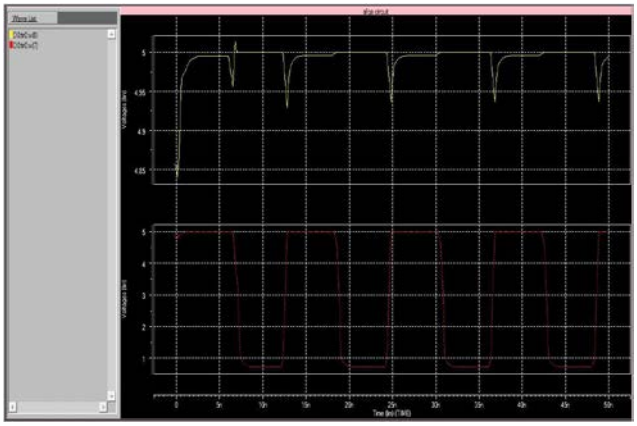

Figure Output waveform of sense amplifier with AFGA

VI. CONCLUSION

A study of various sense amplifiers, Autozeroing floating gate amplifier and noise reduction in sense amplifier with the help of AFGA has been carried out and analog solution is given to reduce offset in sense amplifier. In basic circuit of sense amplifier input transistor are modified to floating gate by adding one capacitor to between bitline and gate. Another capacitor is added between gate and drain, because of these added capacitor input transistor of sense amplifier start working as autozeroing floating gate amplifier. These sense amplifiers and autozeroing floating gate amplifier have been designed in 180nm CMOS technology.

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