Study of A Low Power Pipelined ADC Design

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Abstract- This paper describes the design of first stage of 20-bit, 40-Msample/sec pipeline analog to-digital converter (ADC) is presented. A power consumption of 98 µW was achieved by using low power OTA and switched capacitor MDAC pipelined architecture. This circuit was designed and simulated with the supply voltage of 1.8 V with 65 nm CMOS technology. The proposed design can be a solution for high-speed, low-power applications like portable wireless-LAN cards.

IndexTerms—Low-power, data converter, pipeline ADC.

I. INTRODUCTION

The new generation of wireless-LAN adapters based on the IEEE 802.11a standard [1] imposes a significant challenge to circuit designers. The wide signal bandwidth demands a high sampling rate for ADCs and DACs, however, the power consumption must be kept low in order to extend the battery life of portable wireless devices. The ADC specifications depend on the receiver architecture. For direct conversion receivers two 20 Msample/sec ADCs are needed, while, for low-IF receivers' only one 40 Msample/ sec ADC might be sufficient. The OFDM modulation used in the IEEE 802.11a standard [1] also demands a high resolution for these converters. At least 10 bits are needed in typical receiver designs in order to avoid an increased bit error rate due to ADC's quantization errors.

The power consumption of state-of-the-art ADCs is onthe order of 50 to 100 mW [2]. This is a significant portion of the total receiver power. One should also take into account that the receiver is active during periods much longer than the transmitter for client devices, so the total transceiver power is directly affected by the choice of the ADC.

There are several types of ADC capable of operating atvideo-rate frequencies. These include flash converters, folding and interpolating converters and sub ranging converters.Flash ADCs are too costly for high resolutionsbecause their complexity increases exponentially with thenumber of bits. A 10 bit flash ADC will require 1023, lowoffset, comparators. The folding and interpolating ADCs use a much reduced number of comparators, but offset specifications are still stringent. In this paper, we will focus on the architecture of the pipelined sub ranging ADCs. These ADCs can use a digital correction technique [3] to deal with comparator offsets, relaxing substantially the comparator design and reducing the total required power.

This paper proposes a design technique for pipelinedADC that allows the use of high-speed,low-power, Gm based amplifier and a technique to design sample and hold stage capacitor sharing and design of MDAC. The prototype is designed using 65nm CMOS process on LT spice tool.

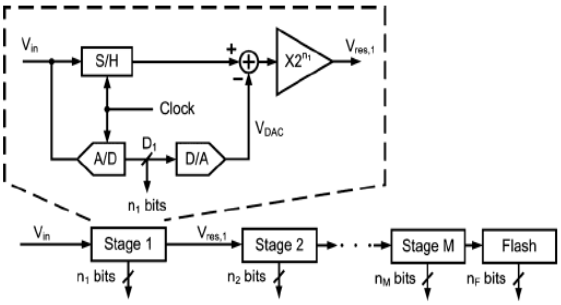

Fig.1.1 Basic architecture of pipeline ADC

Following this introduction, Section II describes theADC's architecture. Section III details the CMOS implementationof its building blocks. Results from Monte-Carlo and transistor-level simulations are presented in SectionIV and experimental results are provided in section V.This paper ends with the VI section.

II. ADC ARCHITECTURE

The basic architecture of pipeline ADC is represented in figure 1 .The pipeline ADC offers the optimal tradeoffbetween conversion speed and resolution; so that it is highly used in application related to high speed and low power. It has an n-bit quantization by cascading digitization stages .Each stage has sampler,ADC, DAC and amplifier.DAC and amplifier are typically called the multiplying-DAC (MDAC).

The ADC presented in this paper is based on switchedcapacitor(SC) circuits. These circuits can achieve verygood accuracy which is a key factor for an ADC that cannottolerate relative errors bigger than 0.1%. The drawbackof SC circuits is their requirement for linear capacitors.However, these capacitors are available in most CMOStechnologies as an option.

In Figure 2 a simplified pipeline stage schematic is shown. This schematic shows a differential circuit for clarity, the actual implementation uses fully-differential circuits in order to reduce the effects of supply and substrate noise. Each stage has two comparator, a differential amplifier various MOS switches and some digital circuits. The capacitors for sampling and hold stage have the equal values. Since the chosenADC architecture leaves very relaxed requirements on the comparators thresholds (100 mV precision) the comparators are designed as simple

dynamic latches.The 1.5-bit DAC is basically an analog multiplexer.

The value of the sampling capacitor *Cs* is obtained from noise and matching constrains and it is different for each stage. First, we want a total sampling noise below the ADC quantization noise [4]:

$$2\sqrt{\frac{kT}{c_s}} \ll \frac{1}{\sqrt{12}}\frac{V_{swing}}{2^N i} \quad \ldots\ldots\ldots\ldots(1)$$

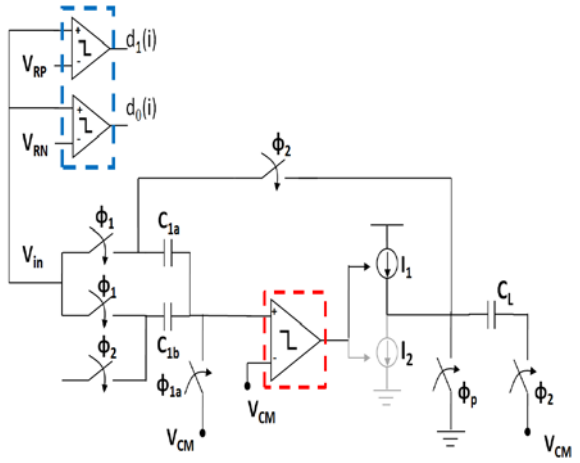

Fig. 2.1 Basic architecture of 1.5 bit stage for pipeline ADC

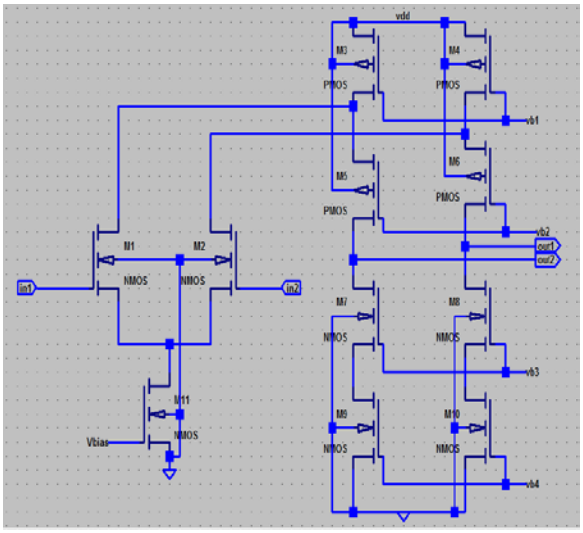

Fig. 2.3 OTA

In this inequality $V_{swing}$is the maximum signal amplitude (2Vref) that is limited by the supply voltage and theoperational amplifier design, N is the number of bits of theADC and i is the stage number. Note that, the minimumvalue of Cs is divided by 4 each time we go to the nextpipeline stage.In this design the sampling capacitance is limited bymatching rather than noise because we still have a highvoltage swing.

III. LITERATURE SURVEY

Pipeline analog-to-digital converters have been extensively used in high-speed medium-accuracy systems due to their partitioned nature. The accuracy partitioning of pipeline ADCs significantly reduces the power and area requirements of a given ADC design, thus allowing designers to push pipeline ADCs to very high speeds.This chapter will cover pipeline ADCs in their most common implementations, as well as established circuit and system design practices for improving the performance of a pipeline ADC. There will also be some discussion on pipeline ADC error sources.

Boris Murmann, Student Member, IEEE, and Bernhard E. Boser, Fellow, IEEE [2003]Presents "A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification"In this In the multibit first stage of a 12-bit 75-MSamples/s proof-of-concept prototype, they achieve more than 60% residue amplifier power savings over a conventional implementation. The ADC has been fabricated in a 0.35µm double-poly quadruple-metal CMOS technology and achieves typical differential and integral nonlinearity within 0.5 LSB and 0.9 LSB, respectively.At Nyquist input frequencies, the measured signal-to-noise ratio is 67 dB and the total harmonic distortion is 74 dB. The IC consumes 290 mW at 3 V.

Dong-Young Chang, Member, IEEE [2004] Presents"Design Techniques for a Pipelined ADC Without Using a Front-End Sample-and-Hold Amplifier "It gives the design techniques for a low-power pipelined analog-to-digital converters (ADCs) without using a front-end sample-and-hold amplifier are presented. Two sampling topologies are compared that minimize aperture error by matching the time constant between signal paths. A digital correction expansion technique is also presented for multibit ADCs, which further increases tolerance to aperture error. Elimination of the front-end SHA can save more than half of the ADCs static power dissipation.

J. Arias, D. Bisbal, J. San Pablo, L. Quintanilla, L. Enriquez, J. Vicente and J. Barbolla [2004] Presents "Low-Power Pipelined ADC Design for Wireless LANs" In this paper a 10-bit, 40-Msample/sec analog to digital converter (ADC) is presented. A power consumption of 12 mW was achieved by using time-interleaved and pipelined architecture with shared operational amplifiers. This circuit was designed for a 2.5-V 0.25-µm technology with metal-oxide-metal capacitors. The proposed design can be a solution for high-speed, low-power applications like portable wireless-LAN cards.

Lane Brooks, Hae-Seung Lee Massachusetts Institute of Technology, Cambridge, MA [2009] Presents "A 12b 50MS/s Fully Differential Zero-Crossing-Based ADC Without CMFB". This paper presents Zero-crossing based circuits (ZCBC) which are used as an alternative architecture where each opamp is replaced with a current source and a zero-crossing detector. This changes the dynamics of the system while preserving the functionality. To further improve the robustness of ZCBC designs, we

present a 50MS/s, 12b ZCBC pipelined ADC with fully differential signaling and automatic offset compensation.

Ashutosh Verma, Member, IEEE, and Behzad Razavi, Fellow, IEEE [2009] Presents "A 10-Bit 500-MS/s 55-mW CMOS ADC" They gives a pipelined ADC incorporates a digital foreground calibration technique that corrects errors due to capacitor mismatch, gain error, and op amp nonlinearity. Employing a high speed, low-power op amp topology and an accurate on-chip resistor ladder and designed in 90-nm CMOS technology, the ADC achieves a DNL of 0.4 LSB and an INL of 1 LSB. The prototype digitizes a 233-MHz input with 53-dB SNDR while consuming 55 mW from a 1.2-V supply.

Jin-Fu Lin, Student Member, IEEE, Soon-Jyh Chang, Member, IEEE, Chun-Cheng Liu, Student Member, IEEE, and Chih-Hao Huang [2010] Presents "A 10-bit 60-MS/s Low-Power Pipelined ADC With Split-Capacitor CDS Technique" In this brief, a split-capacitor correlated double sampling (SC-CDS) technique is proposed to improve the performance of CDS. Using the proposed technique, low-gain operational amplifiers (op-amps) can be employed to implement a low-power pipelined analog-to-digital converter (ADC). A power-efficient class-AB pseudo differential op-amp and its corresponding integrator- based common-mode stabilization (IB-CMS) method are developed to further reduce the power consumption of the ADC. The proposed pipelined ADC fabricated in a pure digital 0.18-μm 1P5M CMOS process consumes 18 mW at 60 MS/s from a 1.8-V power supply.

Chun C. Lee, Member, IEEE, and Michael P. Flynn, Senior Member, IEEE [2011] Presents "A SAR-Assisted Two-Stage Pipeline ADC" They propose a two-stage pipeline ADC architecture with a large first-stage resolution, enabled with the help of a SAR-based sub-ADC. The prototype 12b 50 MS/s ADC achieves an ENOB of 10.4b at Nyquist, and a figure-of-merit of 52 fJ/conversion-step. The ADC achieves low-power, high-resolution and high-speed operation without calibration.

Yunjae Suh, Jongmi Lee, Byungsub Kim, Hong-June Park, Member, IEEE, and Jae-Yoon Sim, Member, IEEE Presents "A 10-bit 25-MS/s 1.25-mW Pipelined ADC With a Semidigital Gm-Based Amplifier". They propose a semidigital Gm-based amplifier for a low-power pipelined analog-to-digital converter (ADC). The amplifier performs a class-AB operation by smoothly changing between a comparator-like semidigital driver and a continuous– time high-gain amplifier according to the input voltage difference. A 10-bit pipelined ADC with 2.5 bit/stage architecture is implemented in a 0.13-μm CMOS. The ADC consumes 1.25 mW at a sampling rate of 25 MS/s and achieves a Nyquist-rate figure of- merit of 139 and 232 fJ/c-s without and with power consumption from a resistor ladder, respectively.

Manas Kumar Hati Tamn K. Bhattacharyya Presents "Design of Low power Parallel Pipeline ADC in 180nm standard CMOS Process". In this paper, design methods of Sample and Hold (S/H) circuit are discussed and gm/id method in OTA (Operational Transconductance Amplifiers) design is applied. Based upon the discussion, circuit design develops from the signal modeling, which would make circuit design concisely and easily. This work is elaborated in details by TSMC 0.18μm CMOS process. Folding telescope structure is applied for main OTA design, with two gain-boost OPAMPs, in order to achieve high gain and high GBW.

IV. CONCLUSIONS

The detailed study of above techniques is done and the merits / demerits are listed under respective headings. Each technique is has its own advantages and disadvantages. So it is better to choose the technique based on the CMOS Technique.

In order to improve the linearity for high-frequency, continuous-time inputs a SHA must be inserted before the ADC.Alternatively, the switches of the first pipeline stages can be replaced with highly linear, bootstrapped switches. The matching between pipelines and the linearity of the ADC can be improved by using INL correction.

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