Power Efficient Architecture for Weighted Partitioning for Multiplierless MCC Circuit with PASTA

Saim Malik[1], Sharad Mohan Shrivastava[2]

[1]Mtech. Scholar, [2]Reearch Guide

Department of Electronics and Communication Engineering, SISTEC, Bhopal

Abstract - An FPGA can be configured and reconfigured for different applications which provide precise timing and synchronization, simultaneous execution of parallel task, and rapid decision making. The complete removal of the multiplier circuitry is by far the preferred choice of circuit designers. The distributed arithmetic (DA) method can be successfully applied in order to partition multiplications in simpler shifts and additions. The partitioning method allows conveniently premultiplying 32-b floating-point filter coefficients with the smallest set of parts composing an unsigned integer input. In this workimproved partitioning method for natural numbers by weighted theory is improved with efficient multiplier using parallel self-timed adder (PASTA), which significantly reduces the power consumption of the application.

Keywords - Multiplierless MCC, PASTA,Weighted Partitioning,parallel processing, distributed arithmetic.

I. INTRODUCTION

Scaling of transistor geometries have led to integration of millions of devices in a very small space, thus driving realization of complex applications on hardware and supporting high speed applications. While the basic principles are largely the same, the design practices have changed enormously because of the increases in and transistor budgets and clock speeds, the growing challenges of power consumption , and the improvements in productivity and design tools. Device scaling has increased the operating frequency of many applications, but has led to high power consumption. This incredible growth has come from steady miniaturization of transistors and improvements in manufacturing processes. Most other fields of engineering involve tradeoffs between performance, power and price. However, as transistor become smaller, they also become faster, dissipate less power and are cheaper to manufacture. This synergy has revolutionized not only electronics, but also industry at large. In order to reduce power, many researchers, designers and engineers have come up with many innovative techniques and have patented their ideas. Nevertheless, designers will need to budget and plan for power dissipation as a factor nearly as important as performance and perhaps more important than area. Low power techniques have been successfully adopted and implemented in designing complex VLSI circuits. As the demand for faster, low cost and reliable products that operate on remote power source performing high end applications keep increasing, there is always a need for new low power design techniques for VLSI circuits. The VLSI designer's challenge is to engineer a system that meets speed requirements while consuming little power or area, operating reliably, and taking little time to design. In this work, low power techniques at circuit level, sub-system level and architecture level are addressed. A power efficient architecture for weighted partitioning for multiplierless MCC circuit with PASTA is designed and implemented by adopting novel low power techniques.

There are many hand-held products that include digital signal processing (DSP), for example, cellular phones and hearing aids. For this type of portable equipment a long battery life time and low battery weight is desirable. To obtain this the circuit must have low power consumption and high speed.

The main issue in this work is to minimize the energy consumption per operation for the arithmetic parts of DSP circuits, such as digital filters. More specific, the focus will be on single- and multiple-constant multiplication using serial arithmetic. Different design algorithms will be compared, not just to determine which algorithm that seems to be the best one, but also to increase the understanding of the connection between algorithm properties and energy consumption. This knowledge is useful when models are derived to be able to estimate the energy consumption. Finally, to close the circle, the energy models can be used to design improved algorithms.

FIR filters can be implemented with multiplier blocks through the use of Multiple Constant Multiplication (MCM). MCM replaces constant multiplications by adders and shifts. Shifts can be hardwired in implementations so the final cost of the design can be measured by the number of adders/subtractors. For longer filters where constant multiplication turns out more bulky MCM makes such

designs simple. There are several algorithms to solve the MCM problem.

II. PASTA ADDERDESIGN

A parallel self timed Adder PASTA is a simplest adder consists of a half adder, a multiplexer and completion detection unitwith avery less number of interconnections. The continuous addition of sum and carry bit in next step simultaneously make it parallel. Asynchronous means the signal indicates the simple data protocols with complete instructions. Self time means, it measures the time spent inside the system automatically performing repeating actions.Adders play a major role in digital circuits. There are three possible operations performed duringbinary addition, the first three produce the sum and rest one is carry generation.Figure 2.1 shows the general architecture of a PASTA adder.

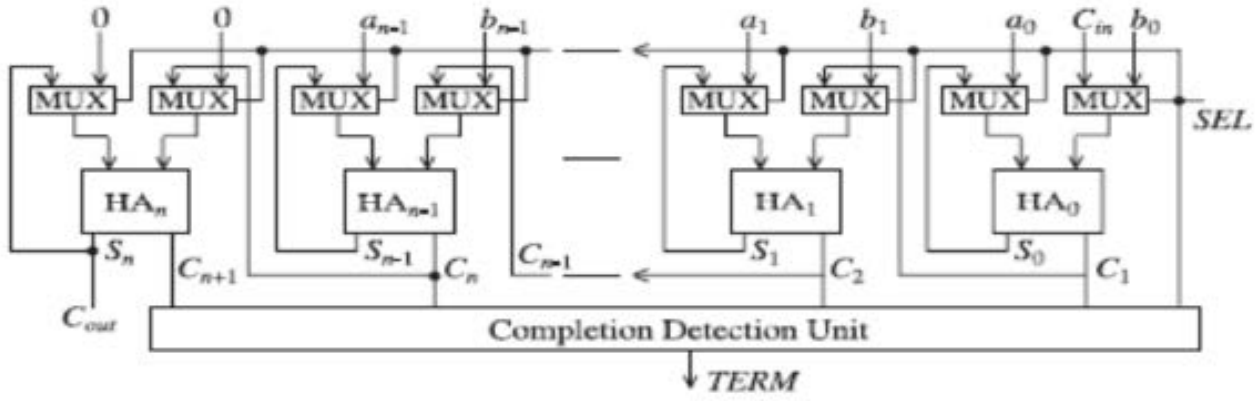

Figure 2.1 General Architecture of a PASTA adder.

The state diagram of a PASTA adder is shown in figure 2.2. There are two state diagrams are plotted (a) for the initial phase and (b) for the iterative phase. The state notation (C_{i+1},S_i) represents the corresponding state of C_{i+1}, carry out and S_i, represents sumvectors for i^{th} bit adder block. During the initial stage, the PASTA circuit works as a combinational HA operates in fundamental mode. It is apparent that due to the use of HAs instead of FAs.

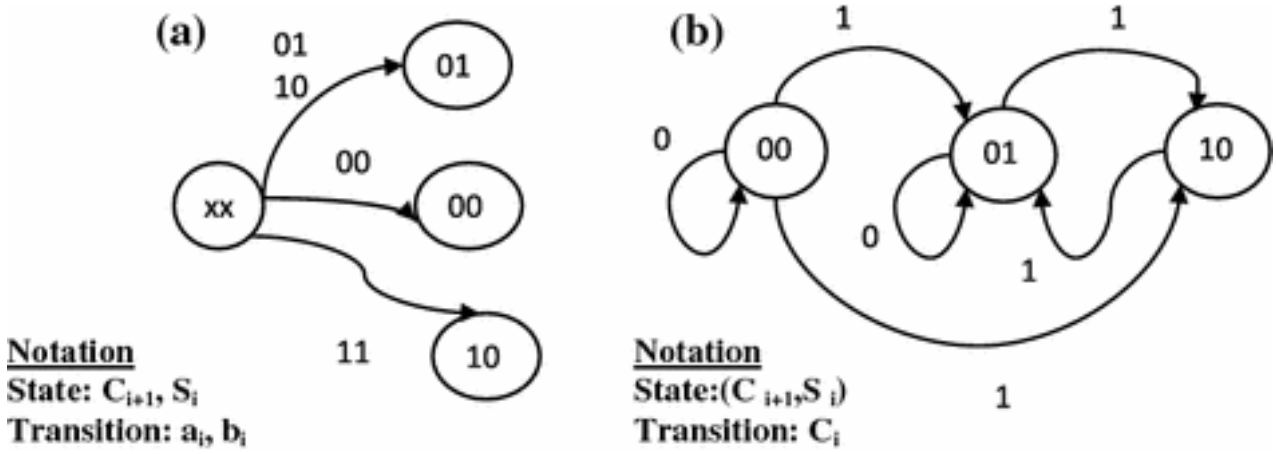

Figure 2.2 State diagram of PASTA adder.

III. PROPOSED METHODOLOGY

To overcome the complexity of arithmetic calculations in a Multiplierless MCC a power efficient architecture for weighted partitioning for multiplierless MCC circuit with PASTAhas reported in this work. An Asynchronous Parallel Self-Timed Adder (PASTA) isutilized to enhance the performance of proposed MCC design due to its wide variety of high speed less complex circuitry. The design of PASTA is uses half adders along with multiplexers requiring minimal interconnections. The design works in aparallel manner for the independent carry chain blocks. The parallel processing property of PASTA adder raises the speed of circuit. AGraph Partitioning is an important problem since it finds extensive applications in many areas. One important application is the reordering of sparse matrices prior to factorization is used to design proposed Module. Theimplementation and execution of proposed work has done on Xilinx ISE design suit and ISIM HDL simulator. The device family used for the implementation of proposed design is a Virtex-7 device family.Top module of proposed architecture has shown in figure 3.1. There

are 12 input output ports are there to design a 32 bit multiplier less multiple constant convolution circuit.Figure 3.2 Sub-modules of Proposed Architecture. The RTL schematic of proposed architecture has been shown in figure 33.

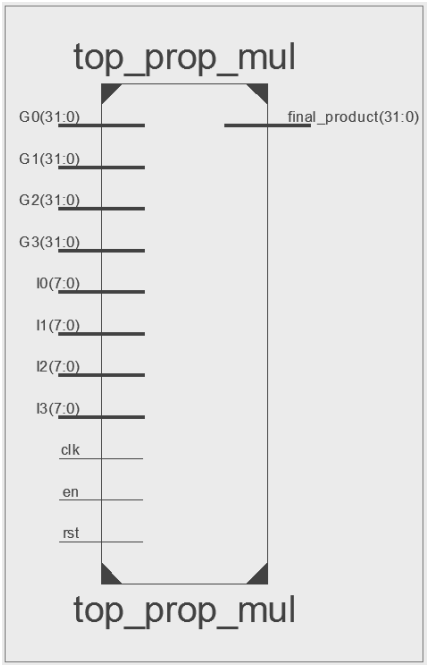

Figure 3.1 Top Module of the Proposed Architecture

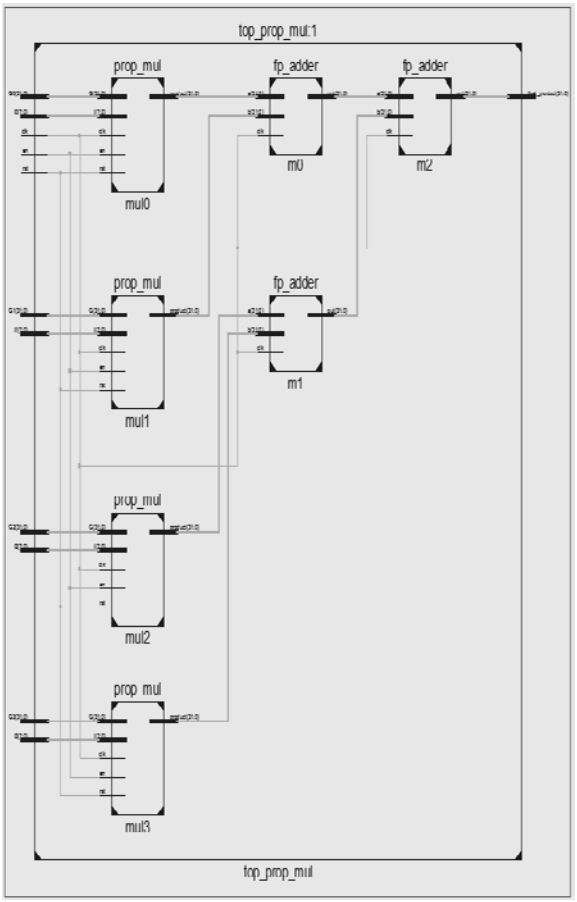

Figure 3.2 Sub-modules of Proposed Architecture.

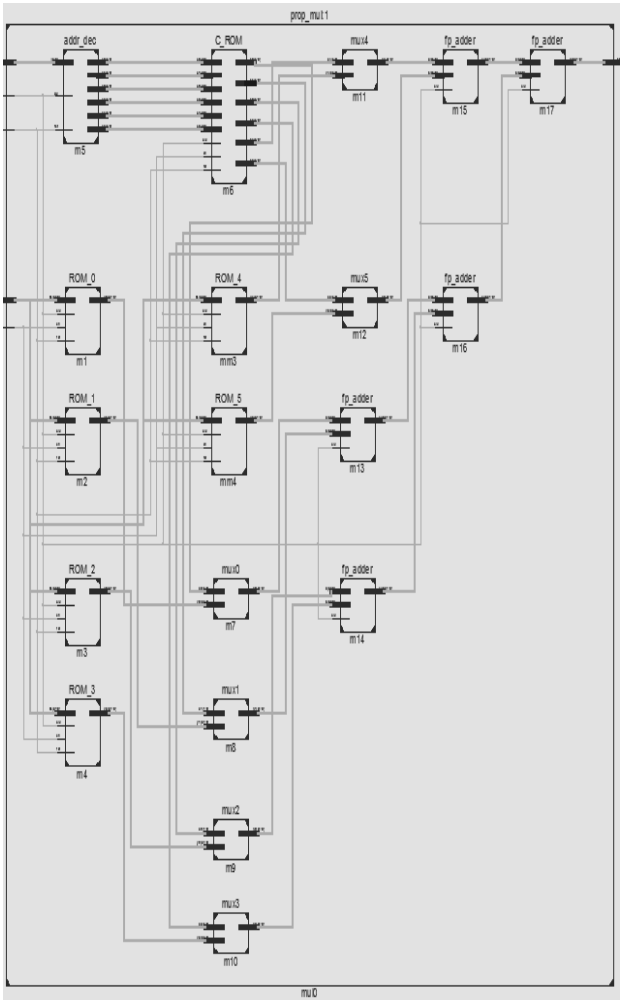

Figure 3.3 RTL schematic of proposed work.

IV. SIMULATION RESULTS

Simulation of proposed work has done on Xilinx Isim Simulator. The simulation screen Xilinx ISE has given in figure 4.1. Figure 4.1 shows the device utilization summary of proposed work in terms of area in number of slices IO buffers.Number of slice registers used 4976 out of 357,600 about to 1% of resource utilization.Number of flip flops used is 3,580 and latches 1396. Number of slice LUTsused is 28427 out of 178,800 available the percent utilization of LUTs is about to 15%. Number of used logics is 28,393 out of 178,800 the percent utilization is about to 15%.Number of used memory is 0 out of 55,600. The main focus of proposed design is to design a power efficient circuit. The power utilization of proposed work has given in figure 4.2 carried out using xilinx xpower analyzer. The analysis of power is done on Virtex 7 device family part xc7v285t and package ffg 1157 on the basis of simulation. The simulation screen of Xpower analyzer is shown in figure 4.2. The total power consumption of proposed architecture is 0547W. The results obtained from proposed design simulation has compared with existing base work the comparison of results are shown in Table 4.1.

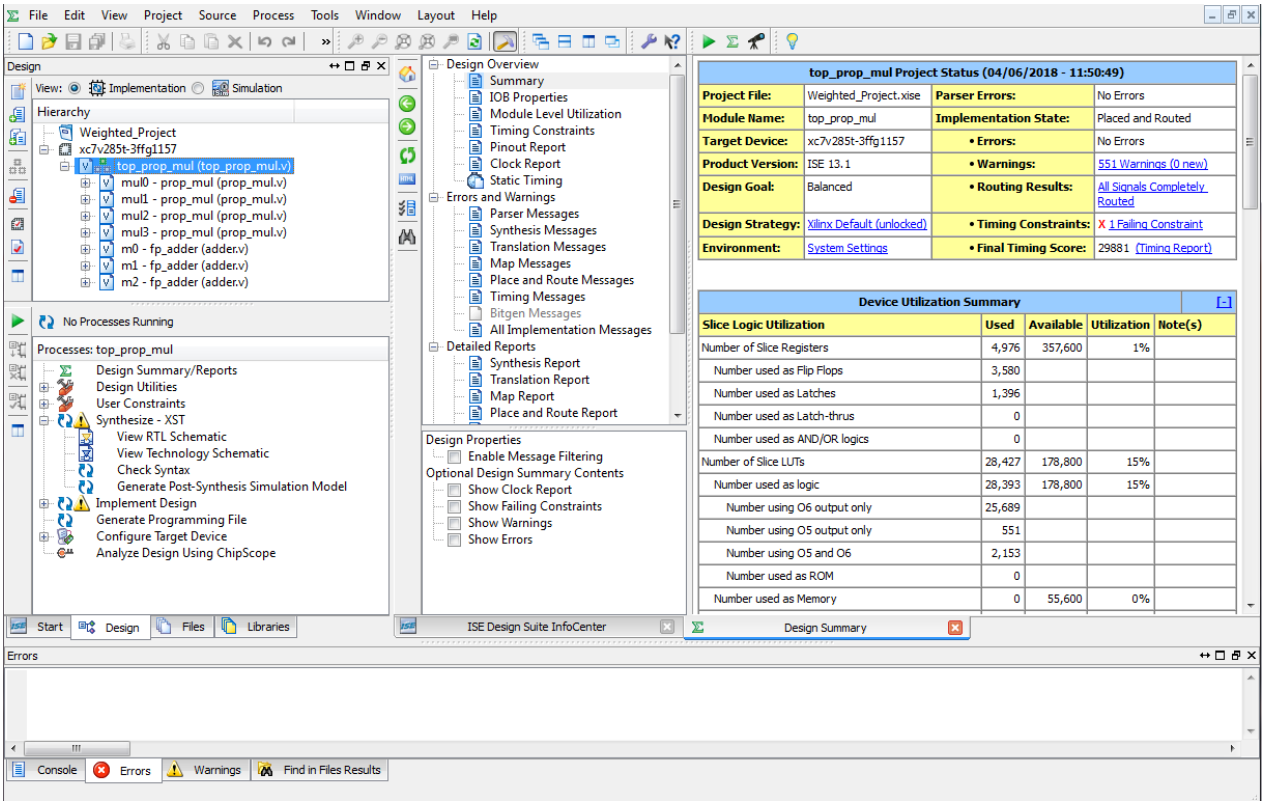

Figure 4.1 XILINX Project View GUI with Device Utilization Summary.

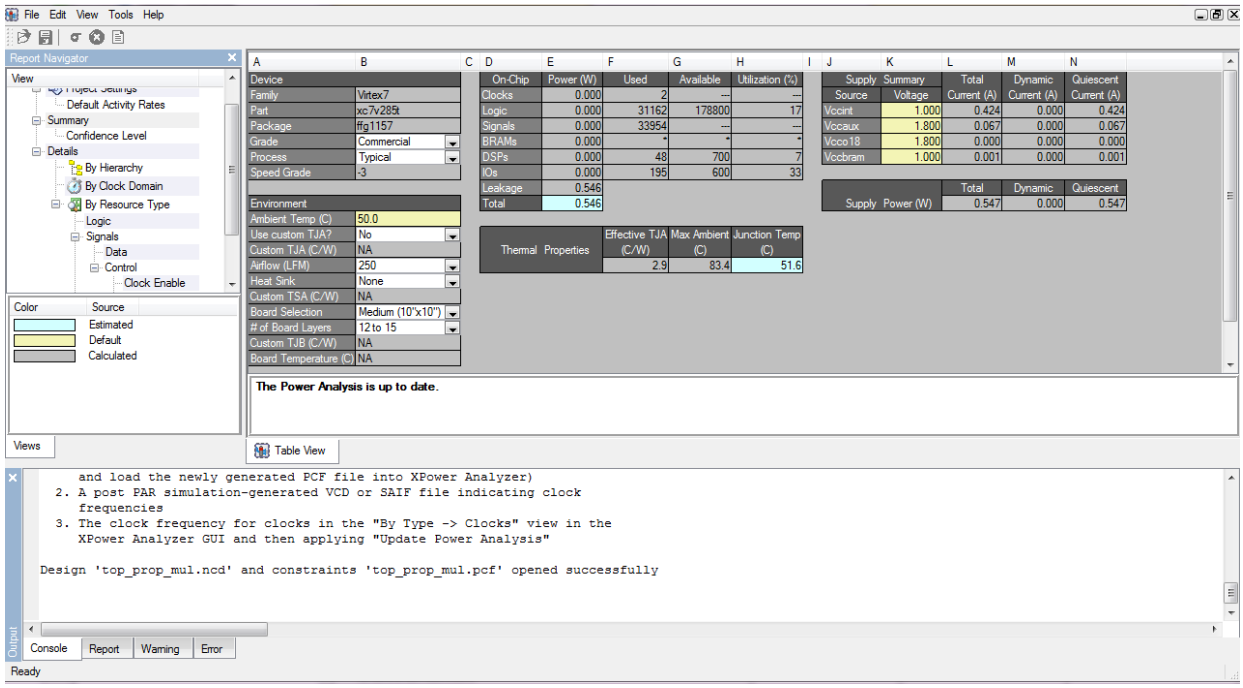

Figure 4.2 XILINX XPower Analyzer - Power Utilization.

Table 4.1 Results comparison.

Parameters	Previous Architecture	Proposed Architecture
Platform	Virtex 7	Virtex 7
Power (W)	2.317	0.547

V. CONCLUSION

Power efficient architecture for weighted partitioning for multiplierless MCC circuit with PASTA has implemented andsimulated in this work on Xilinx ISE and Xilinx ISIm HDL simulator.Research in this field is not only because of the popularity, but also because of the reason that, for

decades the chip size has decreased drastically. This has allowed portable systems to integrate more functions and become more powerful. These advances have also, unfortunately, led to increase in power consumption. This has resulted in a situation, where numbers of potential applications are limited by the power - not the performance. Therefore, power consumption has resulted to be the most significant design requirement in portable systems and this has lead to many low power design techniques and algorithms. In proposed architecture for weighted partitioning for multiplierless MCC circuit with PASTA on the basis of simulation it shows that the proposed architecture ispower efficient as compared to previous work the power consumption of proposed circuit has reduced by2.317 to 0.547W which is a significant improvement in power consumption.

Algorithms used for MCC circuit with PASTA use parallel processing for trade off between various parameters. These algorithms can further be modified to obtain different latencies against variation of other key parameters.

REFERENCES

[1]. G. D. Licciardo, C. Cappetta, L. Di Benedetto and M. Vigliar, "Weighted Partitioning for Fast Multiplierless Multiple-Constant Convolution Circuit," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 1, pp. 66-70, Jan. 2017.

[2]. X. Y. Shih, Y. Q. Liu and H. R. Chou, "48-Mode Reconfigurable Design of SDF FFT Hardware Architecture Using Radix-32 and Radix-23 Design Approaches," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 6, pp. 1456-1467, June 2017.

[3]. Ranjithkumar S and Thilagam S, "Optimization design approach for multiplierless FIR filter," 2016 Online International Conference on Green Engineering and Technologies (IC-GET), Coimbatore, 2016, pp. 1-6.

[4]. I. Sharma, A. Kumar, G. K. Singh and H. N. Lee, "Design of multiplierless cosine modulated filterbank using hybrid technique in sub-expression space," 2016 IEEE International Conference on Digital Signal Processing (DSP), Beijing, 2016, pp. 360-364.

[5]. B. Parhami, "Truncated ternary multipliers," in IET Computers & Digital Techniques, vol. 9, no. 2, pp. 101-105, 3 2015.

[6]. M. Rahman, A. Sanyal and N. Sun, "A Novel Hybrid Radix-3/Radix-2 SAR ADC With Fast Convergence and Low Hardware Complexity," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 5, pp. 426-430, May 2015.

[7]. M. Feilen, A. Iliopoulos, M. Vonbun and W. Stechele, "Weighted partitioning of sequential processing chains for dynamically reconfigurable FPGAS," 2013 23rd International Conference on Field programmable Logic and Applications, Porto, 2013, pp. 1-8.

[8]. F. d. A. T. d. Carvalho and L. D. S. Pacifico, "A Weighted Partitioning Dynamic Clustering Algorithm for Quantitative Feature Data Based on Adaptive Euclidean Distances," 2008 Eighth International Conference on Hybrid Intelligent Systems, Barcelona, 2008, pp. 398-403.

[9]. G. H. Hardy and E. M. Wright, An Introduction to the Theory of Numbers (Sixth Edition). New York, NY, USA: Oxford Univ. Press, 2008.

[10]. S. K. Park, “The r-complete partitions,” Discrete Math., vol. 183, no. 1–3, pp. 293–297, Mar. 1998.

[11]. Ø. J. Rødseth, “Enumeration of M-partitions,” Discrete Math., vol. 306, no. 7, pp. 694–698, Apr. 2006.

[12]. S. Arish and R. K. Sharma, “An efficient floating point multi- plier design for high speed applications using Karatsuba algorithm and Urdvha—Tyriagbhyam algorithm,” in Proc. ICSC, Noidia, India, Mar. 2015, pp. 303–308.

[13]. W. M. Chao and L. G. Chen, “Pyramid architecture for 3840 2160 quad full high definition 30 frames/s video acquisition,” IEEE Trans. Circuits Syst. Video Technol., vol. 20, no. 11, pp. 1499–1508, Nov. 2010.

[14]. M. Potkonjak and M. B. Srivastava, “Multiple constant multiplications: Efficient and versatile framework and algorithms for exploring common subexpression elimination,” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 15, no. 2, pp. 151–165, Feb. 1996.