Low Power Dissipation14bit PipeLine Analog toDigital ConverterUsing 0.18 µm Technology

Dharna Khare, Soheb Munir

Laxmi Narayan College of Technology, Bhopal

Abstract-An 14-bit pipelined analog-to digital converter (ADC) is designed in this paper. The pipelined architecture realizes the high-speed and high-resolution . To reduce some complexities of flash ADC pipeline ADC is used. The calibration schemes of pipelined ADC limit absolute and relative accuracy. Thispaper illustrate a 14 bit 80-Mega bit sample/s ADCmade-up in a0.18 micrometer CMOS technology. The converter employs pipelined Seven stages and implement 2 bit per stage. by using 0.18 CMOS technology.

Keywords:Pipe Line ADC, Amplifier, flash ADC

I. INTRODUCTION

The proposed architecture consists by means of 7 separate 2 bit per stage , 1 DAC block and 1 SHA block with open loop gain of 2. Every block takes equal interval of time to evaluate residue and generate 2-bit of digital output. The focus of this paper will be the power reduction techniques on the architectural level, such as the choice of time alignment and digital correction. The key factor of designing the circuit is to ensure that the all the ADC data conversion ends within the scheduled time interval. Output of ADC is 11, 01 or 00 in thermometer code format. To obtain binary output code the thermometer codes converted by the help of encoder into digital outputs bits 10, 01 or 00 respectively. The resolution each stage is chosen at 2 bit, mainly because of two main reasons, the tolerance on the comparator offset can be as much as ±0.9VREF .There is wide Variety of different ADC architectures available depending on the requirements of the application. Pipeline ADCs are one of the best examples. It typically generate one bit per clock cycle, the Benefits are the low area needed for the implementation. ADCs of this type have good resolutions and quite wide ranges.[14] The ADC is a promising topology for high-speed records conversion with compact area and efficient power dissipation. [15][14][10]

Pipelined ADCs are extensively utilized in the region of military system and wireless communications, digitalized subscriber procession analog frontage ends, monitors, and numerous additional high speed functions. [12][2] The Pipeline ADC realized within this approach is a dynamic come up to merges a flash ADC among the filtrate procedure

Designed used for pipeline accomplishment. a lot of novel thoughts have been implementing to develop the earchitecture such the same as fore-front as well as backdrop Calculations [6][7][8]. This study is arranged as segment II contains mythology. The single step of pipe line ADC is described in segment III. segment IV represents themodel andExperimental outcome are given away in this segment .it is shows various wave form of sub module of single stage pipe line ADC .segment V represent the comparison result of Pipeline design in term of various parameter. Segment.VI represents conclusion and discussions.VII References.

II. PREVIOUS WORK

The design was fabricated using 0.18 µm CMOS technology and the design is implemented in TSMC 0.18µm CMOS technology. Internal flash ADC is 3-bit per stage used which increases the comparator size, thereby increasing the circuit complexity because flash ADC [7] consists of a 2^{n-1} to comparators. Since resolution increases with the comparators size, this pipelined ADC architectures were studied in proposed work. In this work, a 2-bit internal flash is used and resolution & gain have been enhanced. The main objective to design 14 bit pipe line analog to digital converter where each stage consists of two bits and total six stages required to get output of 14 bit.

III. SYSTEM MODEL

As the through put should be as fast as of flash ADC, each stage of the pipeline ADC is inherited form flash structural design. The resolution of each one step will choose how many comparators are set, what will be the latency of the structure This is the motivation, which will simplify the design of other sub-blocks of each stage, For the design of each stage of pipeline ADC), the required components are. Show in fig.1

- Sample and Hold.
- TIQ Comparator.
- 2-bit DAC.
- Amplifier configure for gain of 2.
- Analog Adder.
- Operational amplifier [8]
- D flip-flop
- Encoder

- Analog input

IV. PROPOSED MYTHOLOGY

The this all the subsystem are connected in the cascading form for implementation of pipe line ADC .in this Designed A stage consists of a two bit so total sixstages required to get 14 bit resolution.

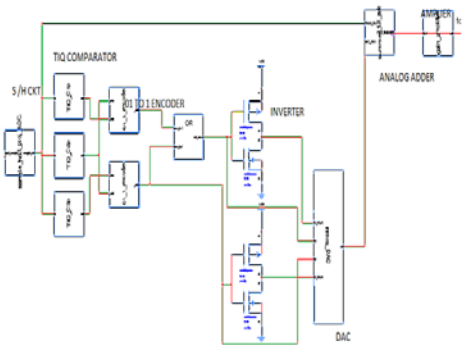

Fig.1 Single Stage Pipeline ADC architecture

A. *Design of Comparator*

Realized flash ADC as aThreshold Inverter Quantization [5] system designed forhigher rate of execution and its smallpower ADC withtypical CMOS toolthisdesign tookeep the necessitate of reference circuit and the comparator will greatly suitable than the conventional comparator because its role to converter analog voltage either logic zero and logic one comparing the reference generator

Show in figure 2mathematically the significance of peak voltage is govern throughmathematically term

$$V_t = \frac{r(V_{dd}-V_{tp})+V_{tn}}{1+r} \qquad r = \sqrt{\frac{Kp}{Kn}}$$

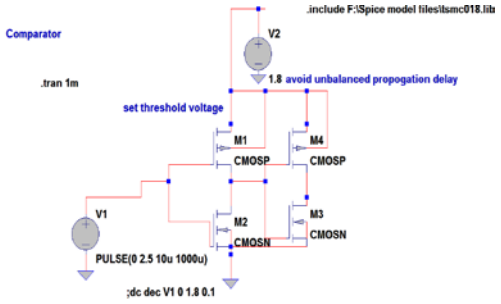

Fig.2 Comparator circuit

B. *Sample and Hold*

SHA plays a vital role in designing the ADC. Once the SHA has converted the input analog signal to the digital time signal, the pipeline can now quantize the held signal accurately without subsidize signal-dependent noise. The drawback of SHA is a momentous increase in power consumption for the whole ADC. Subsequently if SHA block is removed, capacitorsnecessity charge up and hold the signal illustration for significanttimes to consent to the ADC quantized to precisely estimate the changing input signal amplitude. Show in figure.3

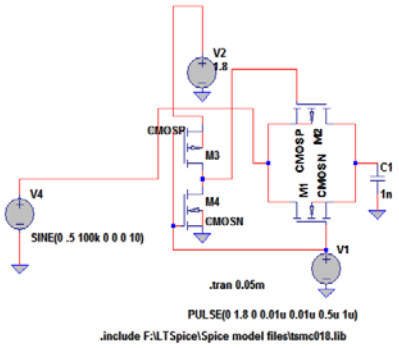

Fig.3 Sample and Hold Circuit

C. *TC to BC Encoder*

TCto-BCencoder utilized because vastly suitable for the ultrahigh speed flashes ADCs. There is flash ADC is well-identified for its high speed process. An n bit ADC's front-end consists of N 1 (where N = 2n)voltage comparators, the main role of encoder in this design to increase the number of bits for the DAC input as shown in Figure 4

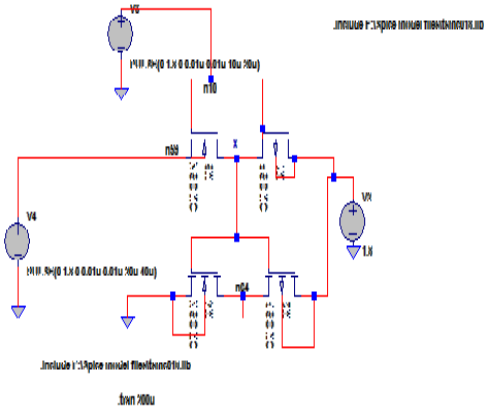

Fig.4 TC to BC converter circuit

D. *Implementation of IGA*

Allpipeline ADC step have single gain stage in this design gainconsists on the numeral of output bits of every onepoint, precisely shown in figure 5

$Av = 2^n$

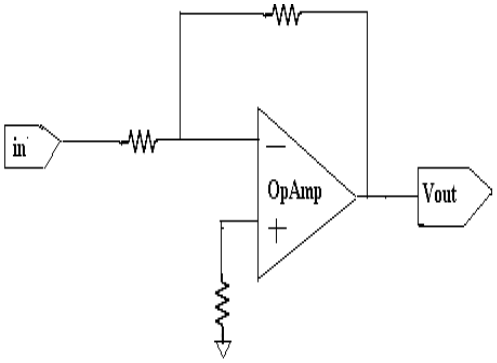

Fig. 5 IGA for Gain Of 4

Somewhere Av is the gain of inverting amplifier and n is the amountof bits of each onestage. Thus the [12] OPAMP has to be configured in closed loop style, since, the proposed design has only one bit per stage, and thus the required gain is 4. The configuration is shown in figure 5

E. ANALYSIS OF D FLIP-FLOP

It is one of mostessentials block in the pipeline ADC, it is utilize as delay constituent which will coordinate the bits of the each and every onestages, withdesigned the flip-flop the same asunreliable length shift register, it will coordinate the analysis of pipeline ADC. Shown in figure 6

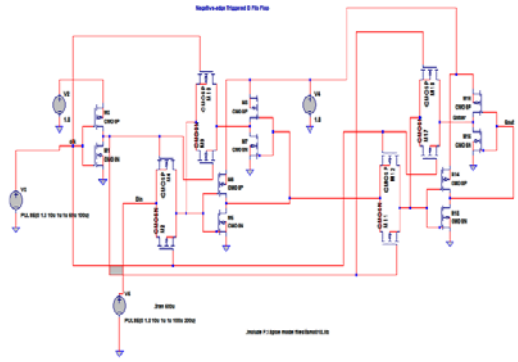

Fig.6 Design of d flip-flop

F. DESIGN OF TWO BIT DAC

Consequently to digitalized CMOS tool, multiplexer logic have been utilize in the direction of act as DAC.[8] the function of DAC is to afford an continuous voltage consequent in the direction ofdigitalized bits, so as tomeans a effortless analog multiplexer be capable of do this trade

The equation recitation the procedure of the Multiplexer that we are with thesame as a 2- bit DAC.Show in figure 7

$$Z = A(S1.S2) + B(S1.\overline{S2}) + C(\overline{S1}.S2) + D(\overline{S1}.\overline{S2}) \quad (1)$$

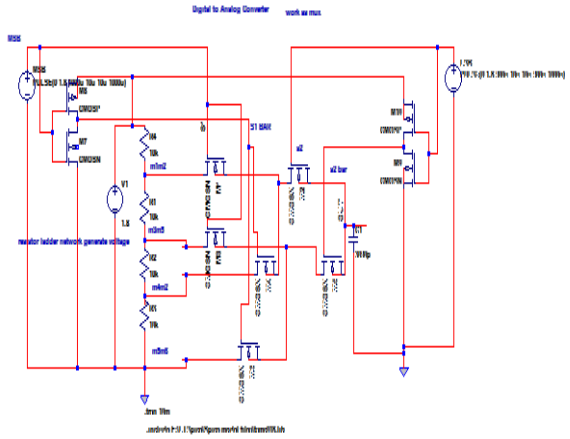

Fig.7Design of Two Bit DAC

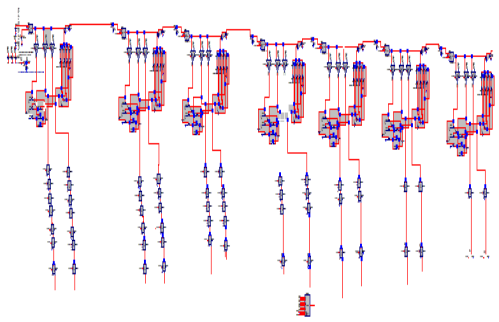

Fig.8 Design of 14 bit pipe line ADC

V. SIMULATION AND RESULT

The design and implementation of 14-bit pipeline ADC has been implemented out on tsmc018micrometer technology, although the proposed of pipeline ADC acquire uncompleted to 14-bit. This is a 0.18micro meter in LT spice switcher CAD-III tool. The supply voltage is bipolar +/- 5(1.8v) the tool used for the design are LT spice switcher CAD-III for schematic, LT -spice for Simulation.

A. Analysis Of Comparator

The direct current experimental result of comparator .the reference voltage is situating at 0.9 volt. thetransitoryoutcome of the comparator show in figure 8 and figure 9

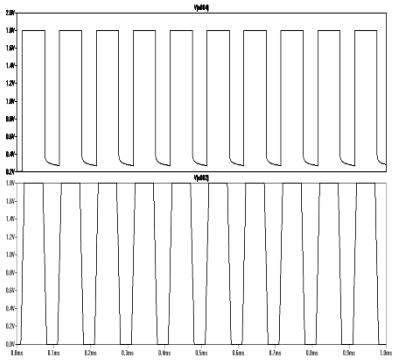

Fig 8Transient Analysis of Comparator

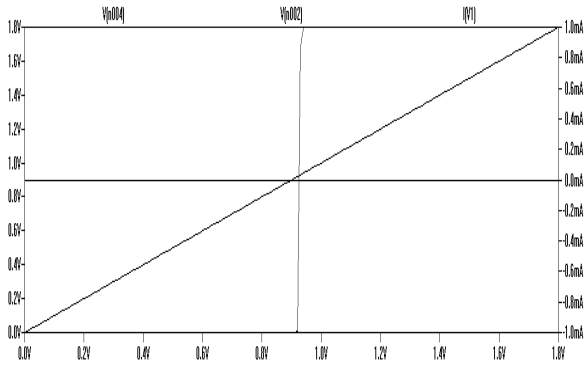

Fig. 9 DC-Sweep Characteristic of Comparator

B. Analysis of Sample & Hold

Experimental result of comparator of the S/H circuit shows in Figure 10

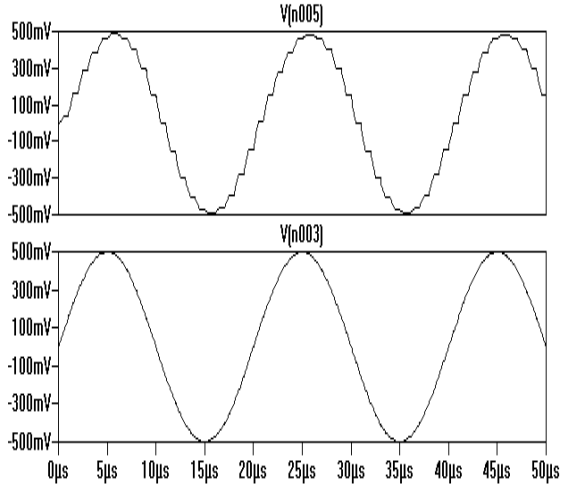

Fig. 10Transient analysis ofS/H Circuit

C. ANALYSIS OF DAC

The transient response of the DAC circuit shows in Figure 11

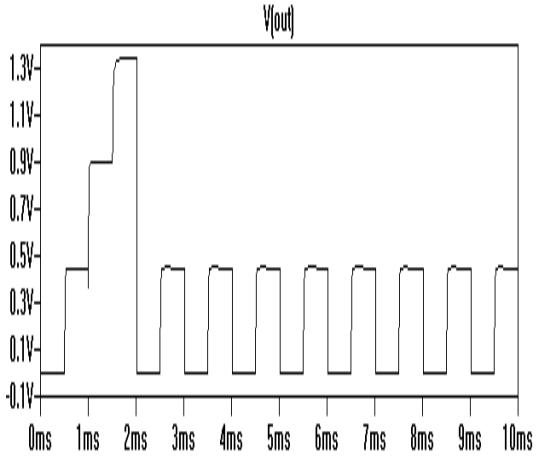

Fig. 11Transient Results of DAC

D. RESULTS OF D-FLIP FLOP

Experimental result of D flips flop shows in Figure 12

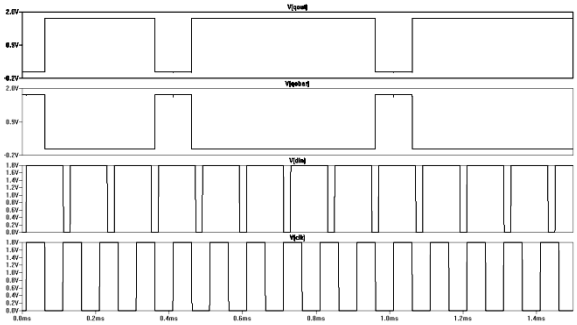

Fig.12 Transient Results of D flip-flop

E. 14 BIT PIPELINE ADC RESULT

Here we will describe how the pipelining is implemented by adding the sub -circuits those we have designed above**.** In first step **to**design pipeline weneed to design Sample & hold circuit, 2-bit ADC,2-bit DAC,and a inverting Gain amplifier. Which we have designed, here we will use four stages to get the resolution of 14-bit.

When we apply the contribution signal to S/H circuit. Get the sampled output as well asthese applied to comparators and get the digital output these digital signal applied to DAC unit to analog signal and output of DAC subtracted to sampled output and amplified by inverting gain amplifier, further applied to second stage. And repeat this steps figure 13 show the seven stage implementation.

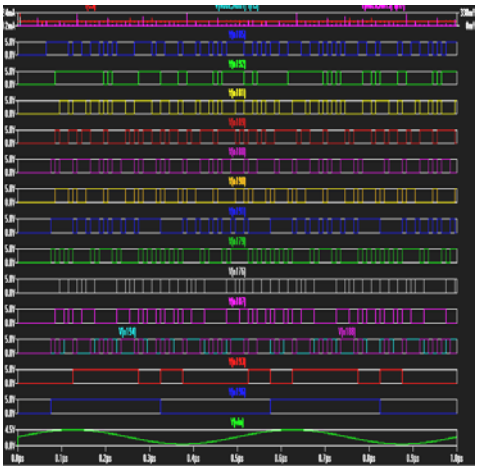

Fig. 13 Transient Results of 14 bit pipeline ADC

VI. COMPARISON

This section show comparison of implementation in term of various parameter shows in below table 1

TABLE 1 COMPARISON TABLE

Parameter	Design 1	Proposed
Sampling frequency	2Ghz	2GHz
Comparator	14	3 per stage
Bit per stage	1.5	2
Power dissipation	22.06Mw	2.0002mW
Full scale input signal	646MHz	10.333MHz
Resolution	8 bit	14 bit

VII. CONCLUSION

The proposed of 14-bit pipeline ADC have been accepted out within TSMC 018µm technology. The proposed is realized in LT Spice Switcher CAD –III Schematic Editor and the outcome isverified through LT spice and simulation analysisinside LT SPICE. The type Design element is reviewed currently. Each block of project is designed at transistor level and design is simulated on LT spice switcher CAD –III schematic editor's simulation tool, schematic editor is used for design entry. The

simulator after simulation provides respective waveforms. Theproposed is implemented onto TSMC0.18technology with aspect dimension of 0.18micron. Satisfactory for the specification.Implemented of six stage we get total Resolution of 14-bit, andSupply Voltage Range = -1.8 V to + 1.8Analog. Input Voltage Range = ± 5V

. Maximum Input frequency >55MHz ,Maximum Sampling rate 20 GHz .and Unity gain inverting Amplifier is to be designed to prove buffering in Sample and Hold stage. DC Gain is 1 V/V. total Power Dissipation is 2.0002mW Technology of design TSMC 0.18 µm CMOS.full scale input signal is 10.333MHz.

FUTURE SCOPE

Because of convergence problem occurring in the tool only 14-bit design of ADC is carried out. The 14-bitpipeline ADC is functioningup and about to 1 GHZ input frequencies. The aim of the project is to design a 14-bit pipeline ADC Design parameters include input range, conversion speed, resolution, power consumption, physical dimensions, etc. This proposed is not targeted to one individualfunction, consequently the design conditionfor various applicationstandards.

REFERENCES

[1] A Pipeline ADC for Very High Conversion Rates Dante Gabriel Muratore, Edoardo Bonizzoni, Franco Maloberti Department of Electrical, Computer and Biomedical Engineering University of Pavia Pavia, Italy

[2] A 12-bit 20MS/s 56.3mW Pipelined ADC with Interpolation-Based Nonlinea Calibration Jie Yuan, Member, IEEE, Sheung Wai Fung, Kai Yin Chan, and Ruoyu Xu, Student Member, IEEE 2011

[3] Low-Power Pipeline ADC for Wireless LANs J. Arias, V. Boccuzzi, L. Quintanilla,L. Enríquez, D. Bisbal, M. Banu, and J. Barbolla ieee 2004

[4] A 6 BIT 1.2 GSps low power flash ADC IN 0.13um digital cmos Martin clara andreas santner thamos hartig

[5] A Pipeline Analogue to Digital Converter in 0.35 µm CMOS S.W. Ross†, StudenT Member, IEEE, and S. Sinha Member, IEEE 2007

[6] A 7 bit 16MS/s low power cmos pipeline ADC Zhuang zhaodong ,li zhiqug ieee 2011

[7] Behazad Razavi‘Design of Analog CMOS circuit Design’, Tata Mc Graw Hil:

[8] T. B. Cho and P. R. Gray, ‘A 10-bit, 20-MS/s, 35-mW pipeline A/D converter,’ in Proc. IEEE Custom Integrated Circuits Conf., May 1994pp23.2.1-23.2.4 .

[9] phillip E. Allen, Douglas R. Holberg, ‘CMOS Analog circuit Design,’ second Edition Oxford university Press. second Edition Oxford university Press.