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A Review Paper on performance Evaluation of Flip-Flop using Various Techniques

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Abstract*—Power consumption plays an important role in any IC, VLSI design and electronic device. In this paper a literature review of true single phase clocking (TSPC), clock pair shared flip flop (CPSFF) and multi threshold voltage complementary metal oxide semiconductor (MTCMOS) techniques. Among those techniques clocked pair shared flip flop consume least power compare to true single phase clocking flip flop. MTCMOS technique which reduce the power consumption of any electronics device by approximately 40% to 60% than the original CPSFF.

Keywords: - Flip flop, TSPC, CPSFF, and MTCMOS.

I. INTRODUCTION

A flip-flop or latch is a circuit that has two stable states which are known as the "1-state" and the "0-state" and can be used to store one bit of information. A flip-flop is a bistable multivibrator which can be constructed from two NAND-gates or two NOR-gate. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic is a type of logic circuit whose output depend on the present input, past input and previous output. In the other word sequential circuit means only store one bit. Flip-flops(generally edge triggered) and latches are a fundamental building block of digital electronics systems used in integrate circuit (IC), microcontroller, microprocessor and many other types of systems.

Flip-flops or latch means a bistable multivibrator can store only stable information. The circuit can be either simple (transparent or asynchronous) or clocked (synchronous); the transparent ones are commonly called latches. The word latch is mainly used for storage 1-bit elements, while clocked devices are described as flip-flops. Simple flip-flops can be built around a pair of cross-coupled inverting elements: vacuum tubes, bipolar field effect transistors, bipolar junction transistors, digital circuit, and inverting logic gates have all been used in practical circuits. Clocked devices basically used for synchronous systems; such devices ignore their inputs except at the transition of a dedicated clock signal (known as clocking, pulsing, or strobing). Clocking causes the flip-flop to either change or retain its output signal based upon the values of the input signals at the transition. Some flip-flops change output on the positive to negative rising edge of the clock, others on the falling edge. The optimization to minimize area at all costs, has only been secondary to the fixation on increasing circuit speed and again our position is that this should be examined with respect to its effect on power consumption. Some of the techniques that will be presented will come at the expense of increased silicon area and thus the cost of the implementation will be increased.

The desirability of this tradeoff can only be determined with respect to a given market situation, but in many cases a moderate increase in area can have substantial impact on the power requirements. It is clear that if power reduction is more important than increasing circuit clock rate, then the area consumed by large clock buffers, power distribution busses and predictive circuit architectures would be better spent to reduce the power dissipation. The total power consumption per device is the sum of a dynamic component from charging and discharging the capacitance and a static component from the leakage current:

$$P_{tot} = P_{dyn} + P_{stat} \quad (1)$$

$$= arf_c C_L V_{DD}^2 I_{off} V_{DD} \quad (2)$$

In this expression f_c is the clock frequency and ar is the switching probability.

The Clock Divider circuit has found immense application in multiple clock domain (MCD) systems like ASICs, SoC (System on Chip) and GALS (Globally Asynchronous, Locally Synchronous).SoC, which is an IC designed by stitching together multiple stand-alone VLSI designs (called IPs) to provide full functionality for an application [l] has different IP blocks operating at different clock frequency. Clock generation and clock distribution for these MCD systems are the costliest in terms of power consumption

[2].The clock generation system generates different frequencies for the clock domains from the basic crystal oscillator (tens of MHz) using PLLs(as frequency multipliers) followed by Clock Dividers. Hence minimizing the power consumption of the clock divider circuit is a crucial step in the design of Clock generator circuit for MCD systems.

The remainder of the paper is organized as follows: section II surveys various techniques for design a flip flop. Variour type of flip flop design a DSCH tool and verified the layout in MICROWIND in Section III. Show conclusion is presented in Section IV.

II. DESIGN A FLIP FLOP IN VARIOUS TECHNIQUE

In literature review, many techniques are proposed for latches and flip flop. In the electronic circuits clock load has been a major concern for the system and fabrication process. In the CPSFF (clocked-pair shared flip flop) clocked pair is shared between the first and second stage of the circuit when it could be converted as a signal level of combination. The schematic of TSPC flip flop is shown in figure 1. This flip flop is consisting of 3 NMOS transistors and 2 PMOS transistors [1], [2], [3]. MTCMOS is the of the most important low power technique which effectively reduces the leakage power.

III. SIMULATION RESULT

The TSPC, CPSFF and MTCMOS circuits could be drawn by using the DSCH tool and verified by the level of the section in the designed circuit.

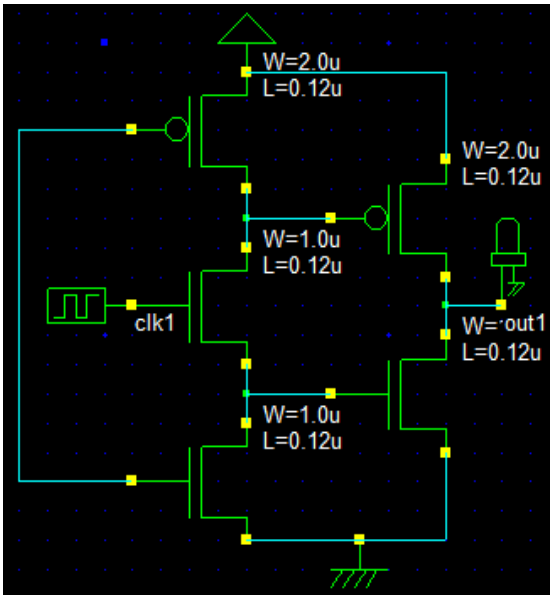

Figure 1: Schematic level for TSPC.

The layout and the compilation could be verified using MICROWIND. DSCH and MICROWIND tools are used to carry out the work for different technologies like 25nm, 65nm and 90nm. The design of TSPC schematics, input output waveform based on DSCH and layout for TSPC based on MICROWIND are shown below figure 1, figure 2 and figure 3 respectively.

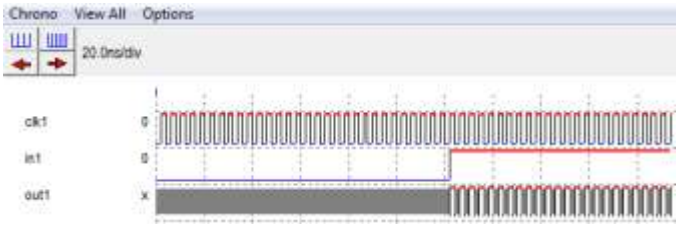

Figure 2: Input output waveform for TSPC.

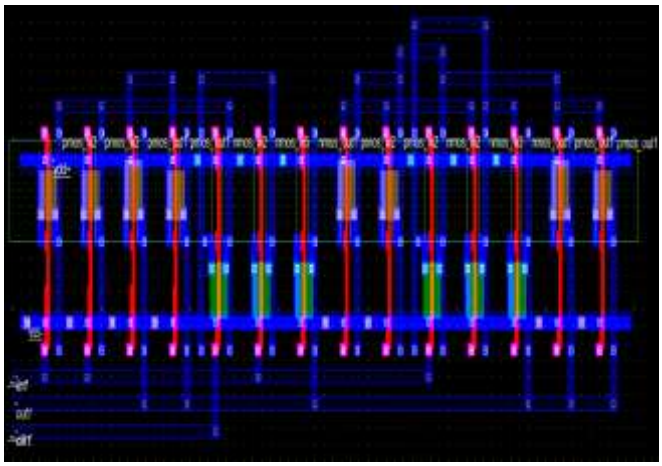

Figure 3: Layout for TSPC

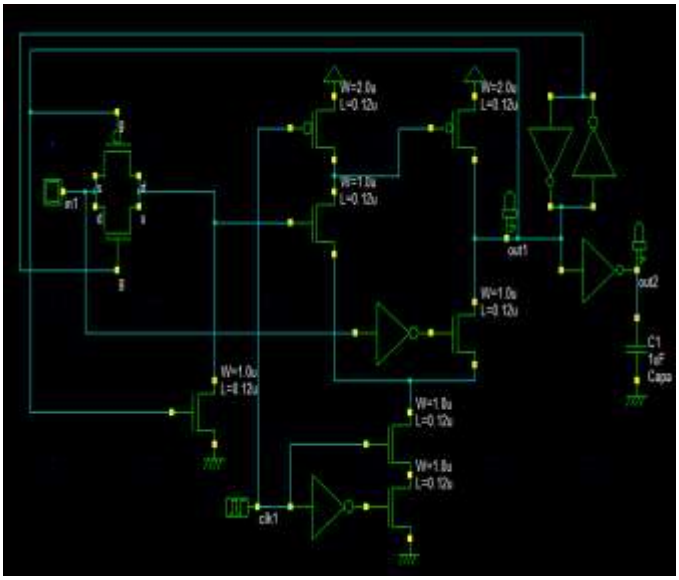

Figure 4: Schematic level for CPSFF.

The design of CPSFF schematics, input output waveform based on DSCH and layout for CPSFF based on MICROWIND are shown below figure 4, figure 5 and figure 6 respectively.

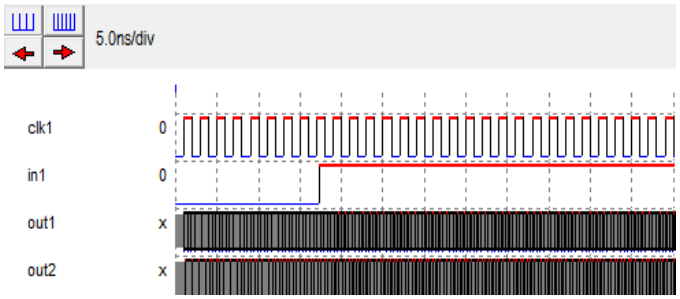

Figure 5: Input output waveform for CPSFF.

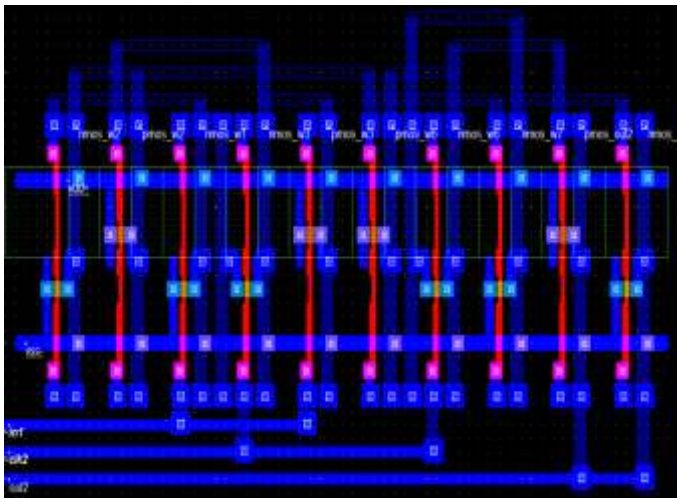

Figure 6: Layout for CPSFF

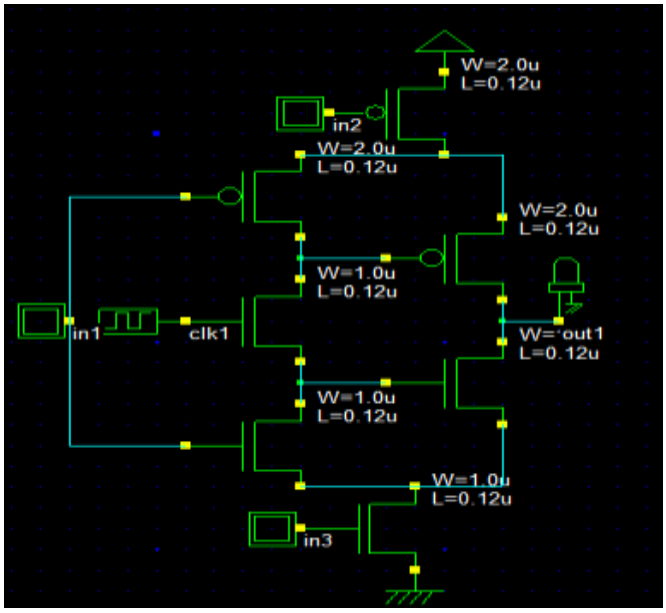

Figure 7: Schematic level for MTCOS.

The design of MTCOS schematics, input output waveform based on DSCH and layout for MTCOS based on MICROWIND are shown below figure 7, figure 8 and figure 9 respectively.

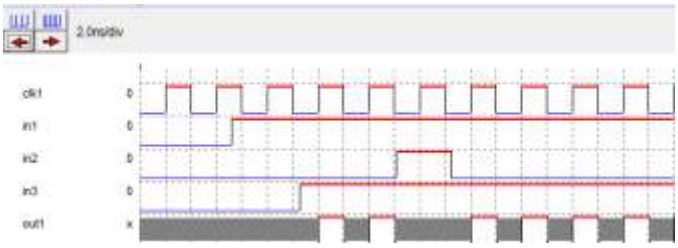

Figure 8: Input output waveform for MTCMOS.

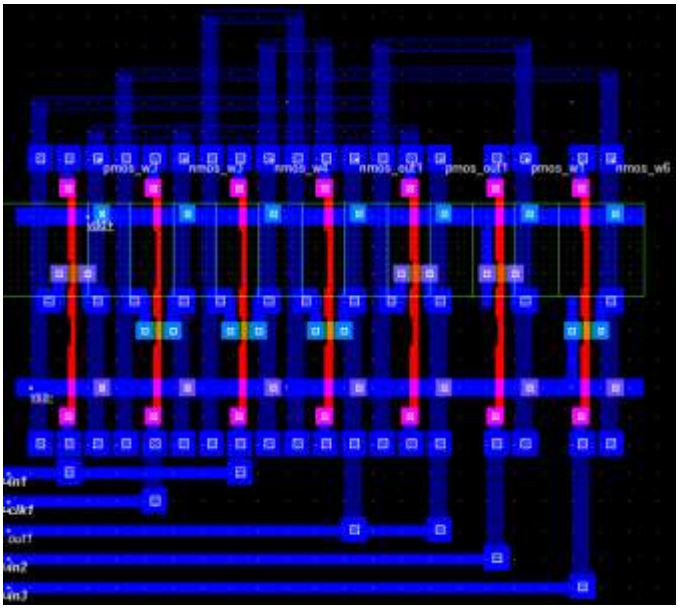

Figure 9: Layout for MTCOS

The comparison between different technologies for TSPC, CPSFF and MTCOS is shown in Table 1.

Table 1: Power dissipation comparisons for different technologies

	Technologies		
	90nm	**65nm**	**25nm**
TSPC	0.835mW	59.49uW	0.947mW
CPSFF	0.734mW	51.32uW	0.754mW
MTCMOS	0.111mW	46.308uW	0.437mW

IV. CONCLUSION

This paper simulated TSPC, CPSFF and MTCMOS designed with different transistor is having different power dissipation.

The flip flops are simulated for 90nm, 65nm and 25nm nodes using the DSCH and MICROWIND tools. Hence from results, as the technologies is scaled down power dissipation increases. MTCMOS are suitable for high performance applications like level converters, microprocessors, clocking system counter etc.

V. ACKNOWLEDGMENT

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