A Novel Design of Low Power consumption 14T Full Adder Circuit

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Abstract- Full adder is the heart of any central processing unit that is a core component employed in all the processors. This paper presents a design methodology for full adder circuit with minimum number of transistor i.e. reduced size & reduced area using CMOS technology. This is then used to implement 14T full adder design for carrying out summation of bits. The analysis of full adder design is done at room temperature CMOS 90 nm technology using Micro wind tool 2.6.The result shows the comparison from CMOS technology in 90 nm using micro wind tool 2.6 on the design in regards of power dissipation, delay and power delay product. We will also provide the layout of the full adder design in 90 nm technology. The proposed technique shows 87.29% less power consumption for FA1 and 86.68% less power consumption for FA2 in 90nm as compare to base paper design.

Keywords: Full Adder, CMOS, DSCH, MICROWIND.

I. INTRODUCTION

Day by day IC technology is obtaining a lot of advanced in terms of style and its performance analysis. A faster speed with lower power consumption and smaller size is implicit to the trendy electronic styles. Full adder usually has extended latency, large space and consumes substantial quantity of power hence low-power full adder style has become a very important part in VLSI system style. Everyday new approaches are being developed to style low-power full adder at technological, physical, circuit and logic levels. Since the full adder is mostly the slowest part during a system, the system's performance is set by performance of the multiplier. Conjointly full adder designs are the foremost space overwhelming entity during a style. Therefore, optimizing speed and space of a full adder may be a major style issue today. However, space and speed are typically conflicting constraints in order that rising speed leads to larger areas and vice-versa. Conjointly space and power consumption of a circuit are linearly related to. Thus a compromise has got to be exhausted speed of the circuit for a bigger improvement in reduction of space and power.

A higher illustration base effectively indicates to fewer digits. Embedded systems style focuses on low Power dissipation and system-on-chip. A reliable on-chip communication customary is a must in any SOC. This section provides an informative review regarding the designing existing mechanism of full adder combinational circuit.

Energy conversion is needed to represent a change in signal value. If energy exists only in one form, i.e. electric energy, then there is only one irreversible energy conversion from electric energy to heat. To break this one-way conversion, researchers have introduced another energy form, i.e. magnetic field energy, into the digital circuit. If one relates the signal change to the conversion of electric energy to magnetic energy the so-called "energy-recovery" can be realized. This is the method by which the irreversible conversion from electric energy to heat caused by dissipative elements, i.e. resistors, is largely reduced or avoided. The energy conversion from electric field to magnetic field and vice versa implies that circuits should be supplied with AC power. In this case, signals in the circuits should also be alternating quantities. The latter has been extensively used in dynamic CMOS logic, clocked CMOS logic and various domino logics. However, those circuits still rely on DC power, and the energy conversion remains as electric energy to heat. There is need for further study in the case of circuits supplied with AC power. The AC power controls the working rhythm of the circuit and acts as the clock, called the power-clock.

Rest of the paper organize as follows: In the section 2 explain the related work results of various full adder design using different mechanism, problem statement describe in section 3, section 4 describe the proposed design and their mechanism and used simulation tool also, section 5 describe the simulation results of proposed hybrid design, last but not the least discuss the conclusion.

II. RELATED WORK

The analysis [1] introduce that the full adder circuit play a significant role in various VLSI circuits. Therefore, style of associate energy-efficient full adder that operates faithfully in submicron technologies has become a good concern in recent years. Some antecedently designed cells suffer from non-full swing outputs, dynamic consumption and low speed problems. During this paper, 2 high-speed, low-power and full swing full adder circuits are designed in 90-nm CMOS technology. In step with simulation results, the projected circuits have rail to rail output signals. Also, associate improvement of 12%-52%, 7%-48% and 28%-68% has been achieved in delay, power consumption and power-delay product (PDP), severally.

In this paper [2], hybrid logic vogue is adopted to style the total adder. The most objective of this style is to attain Low power and high speed. Hybrid logic vogue used is that the combination of C-CMOS logic (Complementary Metal compound Semiconductor) and Transmission gate (TG) logic. The Circuit was enforced using Micro-wind tool in 90nm and 180nm technology. Performance metrics of power and speed are compared with existing adder styles like typical CMOS adder, Transmission gate adder (TGA) and Transmission operate adder (TFA). Average Power consumption of the projected style is found to be 1.114 μW at 90nm for 1.2V offer and 5.641 μW at 180nm for 1.8Vsupply. Delay within the signal propagation is measured as 0.011ns and 0.087ns for 90nm and 180nm technologies severally. So overwhelming very low power and needs less time than existing styles for a similar testing setting. Power Delay Product (PDP) is calculated as product of Power and delay values signifies energy demand of the look. Projected style needs 71 less energy than TFA and 81 less energy than TGA and 92 less energy than typical CMOS adder.

The analysis article [3] projected that the planning multipliers that are of high-speed, low power, and regular in layout ar of considerable analysis interest. Speed of the multiplier factor will be magnified by reducing the generated partial merchandise. Several tries are created to cut back the quantity of partial product generated during a multiplication method one in every of them is array multiplier factor. Array multiplier factor 0.5 adder are wont to total the carry products in reduced time. Achieving high speed integrated circuits with low power consumption could be a major concern for the VLSI circuit designers. Most arithmetic operations are done using multiplier factor that is that the major power consuming component within the digital circuits. Primarily the method of multiplication is complete in hardware in terms of shift and add operation. The optimization of adder has led to the development in performance of multiplier factor. During this paper, a changed full adder using electronic device is projected to attain low power consumption of multiplier factor. To research the potency of projected style, the standard array multiplier factor structure is employed. The styles are developed using Verilog HDL and therefore the functionalities are verified through simulation using Xilinx. The ASIC synthesis results of the projected multiplier factor shows a mean reduction of 35.45% in power consumption, 40.75% in space, and 15.65% in delay compared to the prevailing approaches.

In trendy applied science and quantum computation [4], reversible logic plays an important role because it has nominal impact on physical entropy. Reversible logic gates have same range of input and output thence power loss because of bit erase operation will be avoided. There are several reversible logic structures which might perform totally different Arithmetic and logic operations as ancient or classical logic structures can do. During this paper, 2 reversible logic structures are projected which might perform operation of addition. These logic structures specifically projected style I and projected style II, generate carry output and carry propagate signal on the idea of 2 reversible logic gates referred to as Fredkin gate and nuclear physicist gate. Performance of projected styles is evaluated in terms of quantum value, constant input, garbage output and delay. It's found that projected style II could be a more sensible choice over projected style I and a few different existing styles.

The Paper [5] mentioned the comparative analysis numerous} Fin-FET based mostly full adder cells designed with various logic designs. The logic designs used for implementation of Fin-FET based mostly 1-bit full adder are Complementary MOS (CMOS), Transmission Gate (TG) and Complementary Pass-Transistor Logic (CPL). The simulations have being done at 10nm, 20nm and 32nm technology node for all full adder cell styles. PTM models for multi-gate transistors (PTM-MG) low power are used for simulations. The performance parameters that were measured, analyzed and compared ar average power, leak power, delay, and energy. It's ascertained that less power is consumed in Transmission Gate (TG) primarily based mostly full adder than the Convention full adder and complementary pass-transistor logic (CPL) based full adder in 10nm technology node. Also, found reduction in delay, EDP, and PDP in TG based mostly full adder compared to different cell styles.

The paper [6] terribly large-scale computer circuit (VLSI) style, supported today's CMOS technologies, face numerous challenges. Shrinking junction transistor dimensions, reduction in threshold voltage, and lowering power offer voltage, cause new issues like high leak current, and increase in radiation sensitivity. As an answer for such style challenges, hybrid MTJ/CMOS based mostly style will resolve the difficulty of leak power and produce the advantage of non-volatility. However, radiation-induced soft error remains a problem in such new styles as they have peripheral CMOS elements. As a result, these magnetic-based circuits ar still susceptive to radiation effects. This paper proposes a radiation hardened and low power magnetic full-adder (MFA) for advanced microprocessors. Scrutiny with the previous work, the projected MFA is capable of tolerating any particle strike despite the elicited charge. Besides, our MFA circuit offers a lower energy consumption in write operation as compared with previous counterparts. They conjointly counsel associate progressive modification to the projected MFA circuit to convey it the advantage of full non-volatility for future nonvolatile microprocessors.

The analysis [7] introduce the answer of the intense drawback of threshold loss that causes non-full-swing at

the out-put of 1-bit full adder, an appointment within which all the transistors ar forced to control in sub-threshold regime is projected during this paper. However this may successively bring further space and delay overhead. During this work, full swing at the output of 1-bit full adder is maintained with reduced space and delay overhead. an extra electrical device operating within the differential voltage mode are substitution the junction transistor that's wont to scale back the brink loss drawback at the output of 9T based mostly full adder as mentioned during this paper. Previous works associated with this domain issues regarding reduction of power of solely 1-bit adder. The work targets power and space reduction of 1/4/8/16 bit adders. Projected adder shows most total power saving of 46.87 attempt to 25.99 alter reference to 8T and 9T adder configurations severally.

This paper [8] present, a 3 junction transistor XNOR gate. The projected XNOR gate is intended using CADENCE EDA tool and simulate using the SPECTRE VIRTUOSO at 180 nm technology. The projected results are compared with the previous existing styles in term of power and delay. It's ascertained that the ability consumption is reduced by 65.19% for 3 junction transistor XNOR gate and 48.11% for eight junction transistor full adder. It's conjointly ascertained that the delay is reduced by 31.82% for 3 junction transistor XNOR gate and 28.76% for eight junction transistor full adder.

This paper [9] proposes the look of a coffee power, high speed, and energy economical full adder using changed Gate Diffusion Input (GDI) and Mixed Threshold Voltage (MVT) theme in 45nm technology. The projected style on comparison with the normal full adder composed of CMOS transistors, transmission gates and Complementary Pass-Transistor Logic (CPL), severally, exhibited a substantial quantity of reduction in terms of average power consumption (Pavg), peak power consumption (Ppeak), delay time, power delay product (PDP), energy delay product (EDP) in addition as junction transistor count and thence area. Pavg is as low as 7.61x10-7 watt whereas Ppeak is as low as 6.21x10-5 watt, delay time is found to be 2.05nano second whereas PDP is computed to be as low as 1.56x10-15 Joule and ADP is evaluated to be as low as three.20x10-24 Js for 0.9 V power offer. The simulation of the projected style has been performed in HSPICE and therefore the layout has been designed in Micro-wind.

In this paper [10] they need designed the total Adder using hybrid-CMOS logic vogue by dividing it in 3 modules so it will be optimized at numerous levels. 1st module is associate XOR-XNOR circuit that generates full swing XOR and XNOR outputs at the same time and have a decent driving capability. It conjointly consumes minimum power and provides higher delay performance. Second module could be a total circuit that is additionally a gate and uses carry input and therefore the output of the primary module as input to get total output. Third module could be a carry circuit that uses the output of the primary stage and different inputs to get carry output. Within the new full adder style we've projected new full adder circuit that scale back the ability consumption, delay between due to hold in and PDP by twelve to 100 percent. Simulations are administrated on HSPICE mistreatment TSMC 0.18 µm CMOS technology.

III. PROBLEM STATEMENT

Performance factors such as power, delay, and layout area were evaluated with the existing designs such as STATIC-CMOS, CPL, Hybrid, and Hybrid CMOS, Aguirre's FA, FA1 & FA2 logic full adder. Due to toughness beside CMOS scaling and transistor sizing with the overhead of high input capacitance and requirement of buffers, the adder is designed using static CMOS. Also this design proves the power dissipation cause due to the stray capacitances and large length interconnects. The circuits design using CMOS logic with large number of transistors and maximum length interconnect tare gradually more existing provider to propagation delay, overall area and power consumption. The main goal of this work is to improve the different function parameters such as power dissipation, path propagation delay and number of transistor used in full adder design compared with the previously existing full adder.

IV. PROPOSED MODULE DESIGN

A low power consumption full adder unit has designed with DSCH tool using 14 transistors. The layout of low power consumption full adder has created on micro-wind tool in 90nm technology and simulate with using Verilog language which has generated in DSCH. In this proposed work, low power consumption full adder circuit has been designed by using CMOS logic. Full adder circuit performed operation addition. The layout has made in micro-wind tool for fabrication and power and waveform analysis of design methodology.

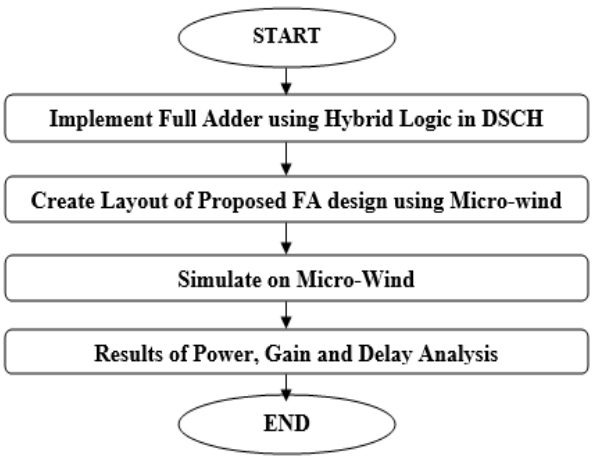

Figure I: Essential Block and Step of Process

Above the figure I show that the essential process block and process involves using of simulation and designing software. Here for this architecture design of 14T full adder used DSCH tool for designing and Micro-wind to obtain power and delay analysis.

In this thesis, an effort towards the design has been made to design and develop the FA circuit by employing single rail lean i.e. transistor logic method. The advantages of CMOS logic come from the fact that it is best suitable to implement power reduction techniques. By eliminating the glitches we can be reduced switching activity in the circuit. This could be done by the delays of each semiconductor unit dominant the widths and lengths. Switch capacitance of a node at intervals the CMOS logic is progressing to be less as compared to a node at intervals the CMOS design as shown in the figure II.

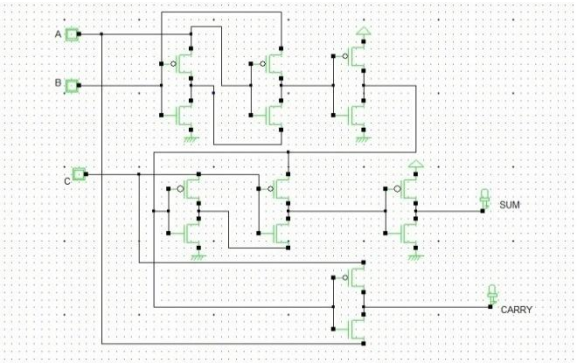

Figure II: Architecture Design of Full Adder Circuit using 14 transistors

V. SIMULATION RESULTS

The proposed full adder with 14T is realized in circuit level with transistor resizing technique as shown in Figure II using DSCH software tool 2.7 and timing diagram shown in the figure IV. Layout level of this design is implemented in 90nm technology using microwind tool 2.6 for delay evaluation as shown in figure V. The design is carried out in 90nm technology to analyze the performance in technology scaling scenarios.

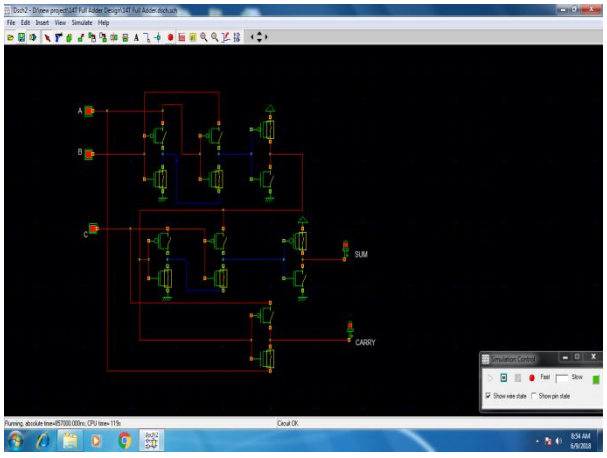

Figure III: DSCH 14 Full Adder Design output Results when all inputs are high (1)

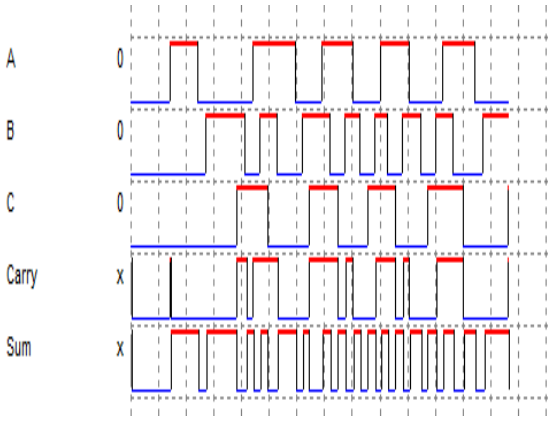

Figure IV: Timing Diagram of DSCH 14T Full Adder Circuit

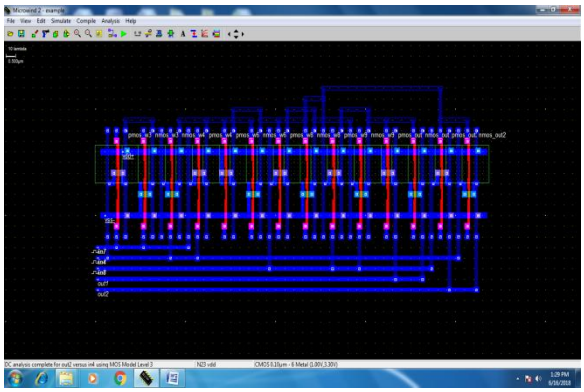

Figure V: Layout of 14T Full Adder Circuit Design in Micro-wind (90 nm)

Table I: Comparison between Base Paper Design and Proposed Design in Terms of Power Consumption for Various Logic Design (1-bit Full Adder)

LOGIC DESIGN	90 nm (power in µW)
CPL	1.88
Hybrid	2.69
Hybrid CMOS	2.71
Aguirre's FA	3.23
Proposed FA1 (Base Paper) [1]	2.13
Proposed FA2 (Base Paper) [1]	1.74
14T Full Adder	0.221

In the table I shows that the average power consumption for various design. In this table we discuss the various designs like STATIC-CMOS, CPL, Hybrid, and Hybrid CMOS, Aguirre's FA, FA1 & FA2 logic and proposed technique and concluded that proposed design shows less power consumption as compare to base paper design.

In the table II shows the % improvement in power consumption for 14T full adder with respect to FA1 & FA2.

Table II: Comparison of Power Consumption and Improvement as Compare to Base Paper Results in Percentage

Power Consumption and Improvement in %				
Method	Base Paper		14T FA	Improvement %
90 nm	FA1	1.74 µW	0.221 µW	87.29
	FA2	1.66 µW		86.68

Summary of Results: In this paper proposed design consist of 14 transistor and using CMOS logic. From discussion of results the following point concluded as below-

- In the table I shows that the average power consumption for various design. In this table we discuss the various designs STATIC-CMOS, CPL, Hybrid, Hybrid CMOS, Aguirre's FA, FA1 & FA2 logic and proposed technique and concluded that the proposed design shows 87.29% and 86.68% less power consumption in 90nm for FA1 & FA2 respectively as compare to base paper design.

VI. CONCLUSION

In this paper proposed design consist of 14 transistors using CMOS logic. From analysis of results concluded that the average power consumption for 14T full adder is less than the existing design. In the table I we discuss the various designs like STATIC-CMOS, CPL, Hybrid, Hybrid CMOS, Aguirre's FA, FA1 & FA2 logic and proposed technique and concluded that the proposed design shows 87.79 % and 86.68 % less power consumption in 90nm for FA1 & FA2 respectively as compare to base paper design.

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