Review Paper on VLSI Architecture of Distributed Arithmetic Based LMS Adaptive Filter

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Abstract-This thesis presents a new area and power efficient VLSI architecture for least-mean-square (LMS) adaptive filter using distributed arithmetic (DA). Conventionally, DA based LMS adaptive filter requires look-up tables (LUTs) for filtering and weight updating operations. The size of LUTs grows exponentially with filter order. The proposed scheme has reduced the LUT size to half by storing the offset-binary-coding (OBC) combinations of filter weights and input samples. To make the adaptive filter more area and power efficient, it is not necessary to decompose LUT into two smaller LUTs. Hence, by using the non-decomposed LUT the proposed design achieves significant savings in area and power over the best existing scheme. In addition the proposed architecture involves comparatively lesser hardware complexity for the same LUT-size.

Keywords-Look Up Table, Distributive Arithmetic Technique, Least Mean Square.

I. INTRODUCTION

The contamination of a signal of interest by other unwanted signal or noise is a problem often encountered in many applications. Linear filters with fixed coefficients are usually used to extract the desired signal where the signal and noise occupy separate frequency bands. Linear filters with fixed coefficients fails to work where signal spectrum overlap with the noise spectrum or the spectral band occupied by the noise varies with time. The filter coefficients need to be changed with time to capture the signal spectrum. The typical applications where fixed coefficients filters are inappropriate are, electroencephalography (EEG) in which signal contamination produced by eye movements is larger than the genuine electrical activity of the brain and share the same frequency band with signals of clinical interest. An adaptive filter is essentially a digital filter with self-adjusting the coefficients according to change in the input signal. Adaptive filter modify its filter coefficient according to the variation in the input signal to estimate the desired signal value using some criterion. Because of its self-adjusting property, adaptive filters are widely used in communication systems, industrial applications and noise cancellation. Few of these applications are discussed here.

Equalization of Data Communication Channels: The channel equalization is widely used technique in digital communication systems. Every pulse propagating through the noisy channel suffers a certain amount of time dispersion because the frequency response of the channel deviates from the ideal response i.e. constant magnitude response and linear phase response. As a result, the tails of adjacent pulses interfere with each other which is known as inter symbol interference (ISI). The ISI can lead to an incorrect decision at the receiver end. Since the channel can be modeled as a linear system, and assuming that the receiver and transmitter do not include any nonlinear operations, the ISI can be removed using linear equalizer. The equalizer function is to restore the shape of the received pulse, as closely as possible, to its original shape. The equalizer transforms the channel to a near-ideal one when its response resembles the inverse of the channel response.

II. LITERATURE REVIEW

M. Tasleem Khan et al. (2018, [1]), an adaptive filter is defined as a digital filter that has the capability of self-adjusting its transfer function under the control of some optimizing algorithms. Most common optimizing algorithms are Least Mean Square (LMS) and Recursive Least Square (RLS). Although RLS algorithm perform superior to LMS algorithm, it has very high computational complexity so not useful in most of the practical scenario. So most feasible choice of the adaptive filtering algorithm is the LMS algorithm including its various variants. The LMS algorithm uses transversal FIR filter as underlying digital filter. This paper is based on implementation and optimization of LMS algorithm for the application of unknown system identification.

Basant Kumar Mohanty et al. (2016, [2]), in this paper, transpose form finite-impulse response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike direct form configuration. In this paper, we investigate the likelihood of acknowledgment of piece FIR channel in transpose frame arrangement for territory defer productive acknowledgment of extensive request FIR channels for both settled and reconfigurable applications. In view of a definite computational examination of

transpose shape arrangement of FIR channel, we have inferred a stream diagram for transpose frame piece FIR channel with upgraded enroll multifaceted nature. A summed up square detailing is introduced for transpose shape FIR channel.

Deepak Kumar Patel et al. (2016, [3]), in this paper, the speed and range are presently the very beginnings of the principal configuration issues in advanced period. To build speed, while doing the duplication or expansion operations, has dependably been a fundamental prerequisite of planning of cutting edge framework and application. Convey Select Adder (CSA) is a quickest viper utilized as a part of numerous processors to fulfill quick number juggling capacity. A wide range of viper engineering outlines have been created to build the productivity of the snake. It is ordinarily realized that every second any processors performed a large number of work works in semiconductor industry. So when we do outlining of multipliers, one of the principle benchmarks is performing speed that ought to be taken in the brain. In this paper, we propose a method for outlining of FIR channel utilizing multiplier in light of compressor and convey select viper. Execution of all viper outlines is actualized for 16, 32 and 64 bit circuits. These structures are integrated on Xilinx gadget family.

K. Durga et al. (2016, [4]), in this paper, an effective engineering of FIR channel structure is exhibited. For accomplishing low power, reversible rationale method of operation is actualized in the plan. Territory overhead is the exchange off in the proposed outline. From the amalgamation comes about, the proposed low power FIR channel engineering offers 18.1 % of energy sparing when contrasted with the customary outline. The territory overhead is 2.6% for the proposed engineering.

IndranilHatai et al. (2015, [5]), this brief proposes a two-step optimization technique for designing a reconfigurable VLSI architecture of an interpolation filter for multistandard digital up converter (DUC) to reduce the power and area consumption. The proposed technique initially reduces the number of multiplications per input sample and additions per input sample by 83% in comparison with individual implementation of each standard's filter while designing a root-raised-cosine finite-impulse response filter for multistandard DUC for three different standards. In the next step, a 2-bit binary common subexpression (BCS)-based BCS elimination algorithm has been proposed to design an efficient constant multiplier, which is the basic element of any filter. This technique has succeeded in reducing the area and power usage by 41% and 38%, respectively, along with 36% improvement in operating frequency over a 3-bit BCS-based technique reported earlier, and can be considered more appropriate for designing the multi-standard DUC.

S. Padmapriyaet al. (2015, [6]), linear phase FIR filter banks form an integral part of the ISO/IEC JPEG 2000 image coding standard. One feature they enable is lossless sub band coding based on reversible filter bank implementations. While this cross sections well with symmetric limit taking care of strategies for entire specimen symmetric (odd-length) direct stage channels, there are blocks with half-example symmetric (even-length) channels, a reality that impacted the JPEG 2000 standard. We demonstrate how these deterrents can be overcome for a class of half-example symmetric channel banks by utilizing grid vector quantization to guarantee symmetry-saving adjusting in reversible executions.

Kiran Joy et al. (2014, [7]), man has achieved wonders in his race from the stone age to the supersonic age. These wonders can be understood from the modern technologies. Technological advancements are becoming a part and parcel of this world. More and more technologies with lot of features and advantages are arising. Reversible logic is one such emerging concept. One of the main characteristics of reversible circuits is their less power consumption. As the technology improves, the number of components and hence the number of transistors packed on to the chip also increases. This causes increase in power consumption. Hence reduced power consumption argued by the reversible logic concept has adequate importance in the present scenario. Reversible logic has a wide application in low power VLSI circuits. This paper aims at promoting the concept of reversible logic by implementing a model of a FIR filter using the reversible Fredkin gate.

Ravi H Bailmare et al. (2014, [8]) exhibited a low power and rapid FIR channel plans by utilizing first request contrast amongst inputs and different requests of contrasts between coefficients. Further, they received the Distributed Arithmetic (DA) design to misuse the likelihood dispersion expecting to lessen the power utilization. The plan was connected to an illustration FIR channel to measure the vitality investment funds and speedup. It demonstrated lower control utilization than the past plan with the similar execution.

M. Usha et al. (2014, [9]) developed a custom Very-Large-Scale Integration architecture, which consists of a reconfigurable hardware substrate and a hybrid-genetic algorithm responsible for resolving the optimal configuration for the reconfigurable components of the substrate. The reconfigurable hardware was specifically tailored for the implementation of multiplier-less symmetrical FIR filters based on the primitive operator technique, while the architecture of the hybrid genetic algorithm aims to improve the quality of the realized filters

and speeding up the time required for their realization. Power analysis demonstrates that the filters, which are implemented by their architecture, consumed considerably less power than industrial Field Programmable Gate Arrays, targeting similar applications.

Sang Yoon Park et al. (2013, [9]) it has been applied for channelizes. Their method was based on the Binary Common Sub-expression Elimination (BCSE) algorithm. The suggested architecture guaranteed minimum number of additions at the adder level and also at the Full Adder (FA) level for realizing each adder needed to implement the coefficient multipliers. Further, they synthesized the architecture on 0.18 m CMOS technology. The synthesis results showed that the proposed reconfigurable FIR filter can operate at high speed consuming minimum area and power. The normal diminishments in region and power were observed to be 49% and 46% individually with a normal increment in speed of operation of 35% contrasted with other reconfigurable FIR channel models in writing.

Basant K. Mohanty et al. (2013, [10]) the CSHM specifically targeted the computation re-use in vector-scalar products and was effectively used in the suggested FIR filter design. Efficient circuit level techniques namely a new carry select adder and Conditional Capture Flip-Flop (CCFF), were also used to further improve power and performance. The suggested FIR filter architecture was implemented in 0.25 m technology. Experimental results on a 10 tap low pass CSHM FIR filter showed speed and power improvement of 19% and 17%, respectively.

H. Thapliyal et al. (2012, [12]), presented three multiplication schemes for the low-power implementation of FIR filters on single multiplier Complementary Metal–Oxide–Semiconductor (CMOS) Digital Signal Processors (DSPs). The schemes achieved power reduction through the minimization of switching activity at one or both inputs of the multiplier. In addition, these schemes are characterized by their flexibility since they tradeoff implementation cost against power consumption. Results were provided for a number of example FIR filters demonstrating power savings ranging from 20% with schemes which can be implemented on existing common DSPs, and up to 51% with schemes using enhanced DSP architectures.

III. SUMMARY OF LITERATURE REVIEW

Summary of literature review shown in Table. In this table used four different types of research paper. All the research paper is used in Xilinx software in different types of device family. In research paper is used in different types of approach and design different types of adder and multiplier using FIR filter.

IV. PROBLEM FORMULATION

In Today's digital word speed is the main concern for higher end applications such as DSP application and embedded application. In these application most of the computing time is consumed by multiplier so multiplier unit need to be less time consuming and more efficient along with speed we have to consider aging effects which hampers multipliers speed.

This century is known as the age of science and technology. The technology is developing very rapidly and the construction and machinery is based on principle of science and math. Math's is in the base of modern invention. However the man is rich or poor, Math's thoughts are on the top of all the process of life of a man. With forthcoming technology, many researchers tried to design multipliers which offer either of the factors high speed, low power consumption, regularity of layout and less area or even grouping of the three in multiplier. Multiplier is the core component of any DSP applications and hence speed of the processor mostly depends on multiplier design. Since multiplication dominates the execution time of most DSP algorithms, so there is a necessity of high speed multiplier. Currently, multiplication time is the dominant factor in shaping the instruction cycle time of a DSP chip [7, 8].

Multipliers and adder are key components of many high performance systems such as FIR filter, narrow band filter, microprocessors, digital signal processors, etc. A system's performance is generally determined by the performance of the multiplier and adder because the multiplier and adder is generally the slowest clement in the system [11].

V. DISTRIBUTED ARITHMETIC TECHNIQUE

Distributed Arithmetic (DA) is a widely-used technique for implementing sum-of-products computations without the use of multipliers. Designers frequently use DDA to build efficient Multiply-Accumulate Circuitry (MAC) for filters and other DSP applications. The main advantage of DA is its high computational efficiency. DDA distributes multiply and accumulate operations across shifters, Look up Tables (LUTs) and adders in such a way that conventional multipliers are not required.

DA Algorithm

Distributed arithmetic is an important algorithm for DSP applications. It is based on a bit level rearrangement of the multiply and accumulate operation to replace it with set of addition and shifting operations. The basic operations required are a sequence of table lookups, additions, subtractions and shifts of the input data sequence. The

Look Up Table (LUT) stores all possible partial products over the filter coefficient space.

Assuming coefficients c[n] is known constants, and then y[n] can be rewritten as follows:

$$Y[n] = \sum c[n]x[n] \qquad n = 0,1,2.....N-1$$

Variable x[n] can be represented by:

$$x[n] = \sum \chi_b[n]2^b \qquad b = 0,1,2.....B-1$$

$$\chi_b[n] \in [0,1]$$

Where the bth bit of x [n] and B is the input width, finally, the inner product can be rewritten as follows:

$$y = \sum c[n]\chi_b[k].2^b$$

$$= c[0](\chi_{B-1}[0]2^{B-1} + \chi_{B-2}[0]2^{B-2} + \chi_0[0]2^0) +$$
$$c[1](\chi_{B-1}[1]2^{B-1} + \chi_{B-2}[1]2^{B-2} + \chi_0[1]2^0) + ...$$
$$c[N-1](\chi_{B-1}[N-1]2^{B-1} + \chi_{B-2}[0]2^{B-2} + \chi_0[N-1]2^0)$$

$$= c[0](\chi_{B-1}[0] + c[1]\chi_{B-1}[0] + c[N-1]\chi_{B-1}[N-1]2^{B-1}) +$$
$$c[1](\chi_{B-2}[1] + ... + c[n-1]\chi_{B-2}[N-1]2^{B-2}) + ...$$
$$c[0](\chi_0[0] + \chi_0[1] + ...c[N-1]\chi_0[N-1]2^0)$$

$$x[n] = \sum 2^b \sum c[n]\chi_b[k] \qquad n = 0,1,2.....N-1$$

Where n=0, 1… N-1 and b=0, 1… B-1

The coefficients in most of DSP applications for the multiply accumulate operation are constants.

VI. VHDL SIMULATION

• VHDL is an acronym for VHSIC (Very high Speed Integrated Circuit) Hardware Description Language.

• VHDL is very adaptive, owing to its architecture, allowing designers, electronic design automation companies.

Parameter:-

• Number 4-input LUTs -LUT stands for look up table that reduces the complex mathematics calculations and provide the reduced processing time.

• Number of Slices -How many areas are used in this circuit is called number of slices.

• Number of IOBs -All input output port used in this circuit are combined called number of input output buffer switch.

• Maximum Combinational Path Delay -How many time of the result is the output of the digital circuit should from level to level are called maximum combinational path delay (MCPD).

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