A Survey and Taxonomy on High Speed Clocked Comparators

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Abstract – Comparators are the basic building blocks of analog to digital converters (ADCs). Comparators are circuits which two analog waveforms and produce an output based on the comparison results. The comparison is however complex based on the fact that it is often challenging to design comparators with high speed, high accuracy and at the same time low power consumption. Comparators are again categorized in to static (unclocked) and dynamic (clocked comparators). This paper presents the basics of comparator design and subsequently presents the design of dynamic comparators with a focus on dual tail comparators. The comparative analysis is based on the power consumption, supply voltage for operation, maximum clock frequency of operation and CMOS technology size. A detailed analysis of the latest dynamic latched with two cross coupled inverters and a total of 9 transistors has been presented and it has been shown that it performs better than double tail latched and preamplifier based clocked comparators. It is expected that the survey will render insights into the design aspects of dynamic comparators paving the path for further research.

Keywords: High speed ADCs, Double-tail comparator, Maximum Clock Frequency, Supply Voltage, Power Consumption, Hysteresis effect.

I. INTRODUCTION

A comparator is basically a circuit that compares two waveforms. The most important application of comparators is in analog to digital converters. Comparators need to fulfill several critical parameters among which the most important ones are high speed, low power consumption, small size and low supply voltage requirement [4] [5]. The basic comparator categories are static (non-clocked) and dynamic (clocked) comparators. Dynamic comparators are generally regenerative comparators with feedback. The feedback path generally connects the input of the comparator and the output of the comparator. The basic comparator action is shown in figure 1.1. In this figure, its is shown that the comparator circuit compares two voltages Vin1 and Vin2. The output is a voltage Vout. Two additional inputs to the comparator are Vcc and ground (gnd). The mathematical condition for the output logic is given by:

$$V_{out} = logic\ 0; for\ Vin_1 > Vin_2$$

$$V_{out} = logic\ 0; for\ Vin_1 < Vin_2$$

The empirical circuit for such a comparator is given by:

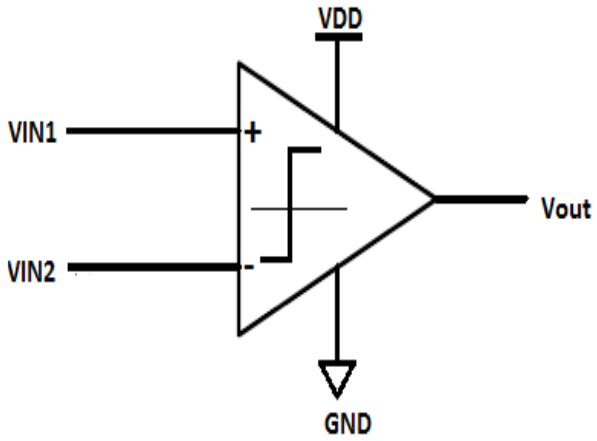

Fig. 1.1 Empirical Block Diagram of Comparator.

A detailed comparison, previous contextual work and working of the comparator is presented in the subsequent sections.

II. CLOCKED RENERATIVE COMPARATORS

As mentioned earlier, the basic categorization of comparators is in the form if clocked and unclocked comparators. Clocked comparators have a feedback mechanism and are called regenerative comparators. [4]The clocked comparators are also called comparators with tail or tailed comparators. A comparator with a single clock is called a single tail comparator and a comparator with two clocks is called a dual tail comparator. A pictorial comparison of the comparators is given in figure 2.1.

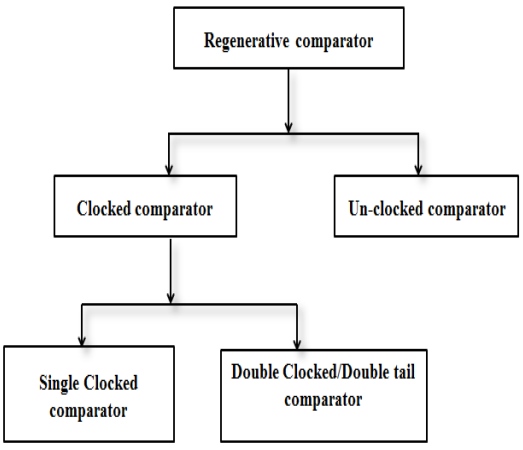

Fig. 2.1 Comparator Categories

The dynamic comparators can be basically categorized into single tail comparator and dual tail comparator.

A. Conventional Dynamic Comparator

The conventional dynamic comparator is basically a comparator with only one clock operating the comparator. [1] The advantage of the clock is the fact that the comparison occurs only at the rising or the falling edge of the comparator. In between, the previous output is held by the comparator. The dynamic comparator's speed of operation is governed by the maximum clock frequency or maximum frequency of the tail. [3] There is a maximum frequency which is supported by the comparator circuit.

B. Dynamic Double Tail Comparator

The dynamic double tail comparator is a modified version of the conventional comparator circuit. In this case, there are generally two clocks in operation in synchronization. The two clocks are called the two tails. [7] The performance of the comparator is evaluated based on speed of operation, power consumption and size. The speed of the dual tail comparator critically depends on the charging time of the load capacitance (Latch Delay). Thus the time period of the dynamic comparator would be the addition of the latching time and load capacitance charging time (latch delay). Mathematically,

$$t_d = t_L + t_c$$

Here,

t_d is the total delay

t_L is the latching time

t_C is the load capacitance charging time

III. PREVIOUS WORK

The detailed analysis of previous work shows that that the speed of operation of clocked (dynamic) comparators depends on the maximum clock frequency. [2] In previous works, it has been shown that propagation time delay, energy per conversion, noise, supply voltage and sampling frequency which are the critical parameters for the performance evaluation parameters for the comparators. An analysis on the performance issues of the prominent comparator designs in presented below.

A. CMOS multistage preamplifier deign for High-Speed and High-Resolution Comparators by Eiji Shirai

In this paper, [9] the authors have included the pre-amplifier stage to obtain satisfactory gain, high speed performance and low power consumption. Conversion rate is investigated to be high by optimizing the trade off the number of stages or number of pre-amplifier stages and the capacitor storage. The noise and gain trade-off has been analysed in the mathematical model for the circuit. The circuit is designed on 400nm CMOS technology with a maximum sampling frequency of 13Msample/s. It can be seen from the output transient analysis that the proposed circuit renders lesser offset.

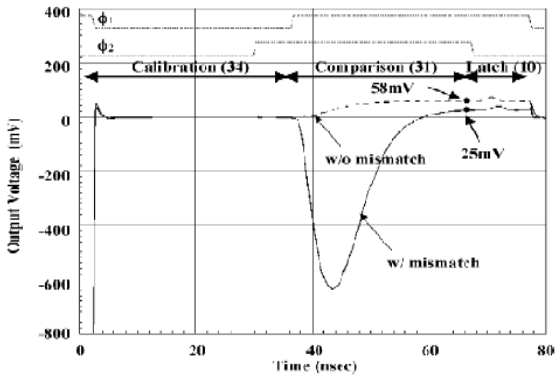

Fig. 3.1 Transient Analysis of [9]

The pre-amplifier stages are successful in reducing the offset of the circuit designed but its power dissipation, energy per conversion and supply voltage still remain a limitation.

B. 40-Gb/s CMOS clocked comparator with bandwidth modulation technique by Yusuk Okaniwa.

In this paper [10], the author propose a clocked comparator with bandwidth modulation with the sub-sections of front end sampler, which samples and latches on to the data, regenerative stage with the feedback action and a clocked amplifier which amplifies the signal from the regenerative stage. This circuit uses a standard CMOS technology and requires a supply voltage of 1.2V. The circuit block level approach is shown in figure 3.2. [10].

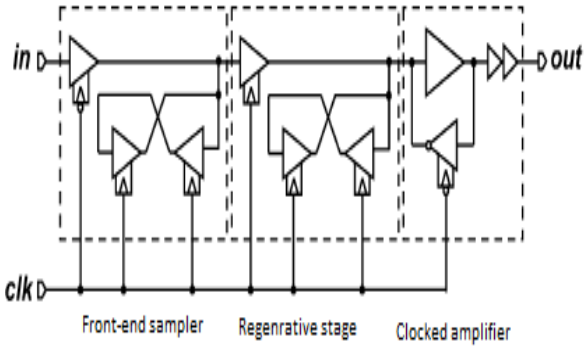

Fig. 3.2 Block level circuit design of [10]

C. Low power and low voltage inverter based double tail comparator by B. Prasanthi

In this paper, [11], the focus was on the delay analysis of the circuit with an addition of an N-MOSFET transistor to reduce the delay and power consumption of the previously existing conventional circuits. The circuit is designed at 250 nm CMOS technology. The results clearly exhibit the

fact that the proposed circuit has a lesser power consumption or energy per conversion.

The limitation however remains the relatively large technology size of 250nm CMOS technology and delay.

D. Analysis and design of a low voltage low power double-tail comparator by Samaneh Babayan-Mashhadi.

In the proposed work [8], the authors designed a comparator on in 180nm CMOS technology, with required supply voltage of 0.8V and a maximum clock frequency of 1.1GHz. The results of the proposed circuit are analyzed in terms of clock frequency, power consumption, and supply voltage and noise effects. The effect of hysteresis effect and kick back noise has also been analyzed. The hysteresis effect is the property of the comparator circuit to hold on to previous output even when the inputs have changed. The effect of noise in the output waveform due to the regenerative effect has been shown. The circuit for the designed circuit is shown below:

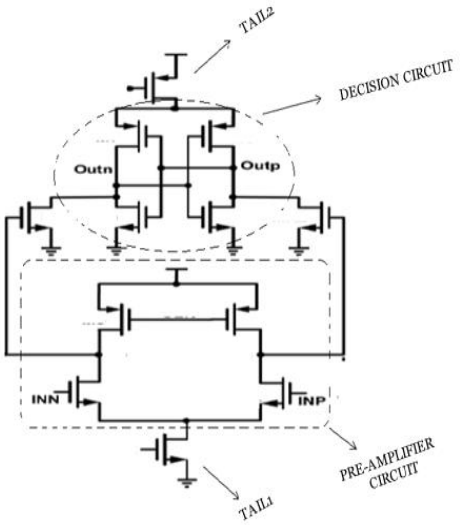

Fig. 3.3 Dual tail comparator of

The results obtained can be visualized using the transient analysis of the circuit as given in [8] and is shown in the figure below.

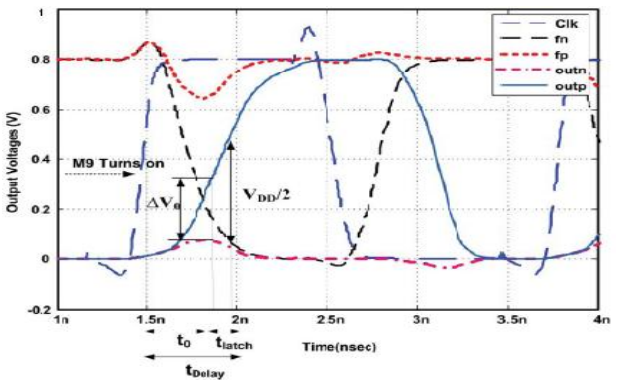

Fig. 3.4 Transient Analysis of [8]

The circuit has the following limitations or scopes for improvement:

- Reduced technology size
- Reduced power consumption or energy per conversion
- Higher clock frequency

A comparative summary of the previously existing techniques has been summarized in TABLE1.

TABLE 1. COMPARATIVE PERFORMANCE SUMMARY

S. No.	Parameters	Previous Work			
		Multistage Preamplifier Design Method	Bandwidth Modulation Technology	Inverter Based Comparator	Double Tail Comparator
1.	CMOS Technology	400nm	110nm	250nm	180nm
2.	Supply Voltage	2.5 V	1.2V	1.5V	0.8V
3.	Maximum Sampling Frequency	13MHz	2.5GHz	1GHz	2.4GHz
4.	Energy per Conversion	20pJ	-	-	24pJ

IV. PROPOSED METHODOLOGY

The proposed methodology can focus on designing an optimized and improved version of the dual tail comparator with the aim of improving the parameters of CMOS technology size, power consumption. Supply voltage and clock frequency. The way in which it can be done is by reducing the delay in the output waveform due to the MOS capacitance effects. The starting phase of the comparison at every clock edge needs the outputs of two CMOS transistors to be closer enough to minimize the delay effects thereby increasing the clock frequency. The channel length can be reduced in order to reduce the transition time of electrons from source to drain thereby increasing the clock speed. This would have a two way effect of reducing the power consumption since the energy per conversion would decrease since the same comparison

operation would be over in lesser time. Thus the parameters to focus upon are:

1) Clock speed

2) Supply voltage

3) Power consumption or energy per conversion

4) CMOS technology size

5) Delay

V. CONCLUSION

It can be concluded from previous discussions that comparators are the basic building blocks of analog to digital converters. The comparison and output of the comparison is however accompanied by several tradeoffs. The major attributes of the comparator are the speed (which should be as high as possible), CMOS technology size (should be as small as possible), Power Consumption (should be as low as possible) and delay (should be as low as possible). A comparative description of the various parameters of the previous work has been summarized with an in-depth analysis of the approach followed. The proposed methodology presents a roadmap for an improved and optimized comparator design.

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