Reduce Area and Delay for Adaptive Filter using Decimation and Interpolation Approach

Anjali Pandey[1], Ms. Kiran Sharma[2], Mr. Santosh Onker[3]

[1]M. Tech. Scholar, [2,3]Assistant Professor,

Department of Electronics and Communication, SAMCET, Bhopal

Abstract:-More and more people around the world suffer from digital signal processing research field. The increase hardware complexity and increase area are the main reasons for this field. The multi-rate approach used for narrow band filter is designed and implemented in Xilinx Vertex-E XCV50E device family. The multi-rate approach is design using the decimator and interpolator structure in VHDL. Each structure is simulated using Xilinx Vertex-E XCV50E device family and compared the existing structure. The resulting structure is hardware efficient and consumes fewer slices compared to existing structure.

Keywords:Filter Coefficient, Finite Impulse Response, Pass-band Frequency, Narrow Band Filter.

I. INTRODUCTION

Multi rate simply means "multiple sampling rates". A multi rate DSP framework utilizes different testing rates inside the framework. At whatever point a flag at one rate must be utilized by a framework that anticipates an alternate rate, the rate must be expanded or diminished, and some preparing is required to do as such. Along these lines "Multi rate DSP" truly alludes to the workmanship or study of changing testing rates. Multi-rate preparing discovers use in flag handling frameworks where different sub-frameworks with varying example or clock rates should be interfaced together. At different occasions multi-rate preparing is utilized to decrease computational overhead of a framework. For instance, a calculation requires k tasks to be finished per cycle. By diminishing the example rate of a flag or framework by a factor of M, the number-crunching transfer speed prerequisites are decreased from kfs activities to kfs/M tasks every second. Customary converters are regularly hard to actualize in scarcely discernible difference huge scale coordination (VLSI) innovation. By remembering these things the general population is going for over examining converters, these converters make broad utilization of computerized flag handling.

- Higher reliability.
- Increased functionality.
- Reduced chip cost.

Those attributes are regularly required in the advanced flag handling condition of today. An essential use of computerized flag handling techniques is in deciding in the discrete-time do-fundamental the recurrence substance of a ceaseless time flag, all the more generally known as unearthly examination. All the more specifically, it includes the assurance of either the vitality range or the power range of the flag.

Practically all melodic projects are delivered in essentially two phases. To start with, sound from every individual instrument is recorded in an acoustically dormant studio on a solitary track of a multitrack recording device.

At that point, the signs from each track are controlled by the sound architect to include unique sound impacts and are joined in a blend down framework to finally produce the stereo chronicle on a two-track recording device.

The sound impacts are artificially produced utilizing different flag preparing circuits and gadgets, and they are progressively being performed utilizing advanced flag handling strategies.

The remainder of the paper is organized as follows: multi-rate approach algorithm is presented in Section II. The proposed structures of narrow band filter are presented in Section III. Hardware and time complexity of the proposed structures are discussed and compared with the existing structures in Section IV. Conclusion is presented in Section V.

II. MULTIRATE APPROACH

The procedure of changing over a flag from an offered rate to an alternate rate is called testing rate transformation. The frameworks which utilize various examining rates in the handling of advanced flag are called multi-rate flag preparing [5].

Annihilation is the procedures of bringing down the word rate of a carefully encoded flag, which is inspected at high frequencies much over the nyquist rate. It is typically done to build the goals of an oversampled flag and to expel the out-of-band clamor. In a sigma-delta ADC, oversampling the simple information motion by the modulator alone does not bring down the quantization commotion; the ADC should utilize an averaging channel, which fills in as a decimator to expel the clamor and to accomplish higher goals. An essential square diagrammatic portrayal of the

decimator is appeared in Figure 1.The decimator is a blend of a low pass channel and a down sampler. In Figure 1 the exchange work, H(z) is illustrative of performing both the activities.

The yield word rate of the decimator is down inspected by the factor M, where M is the oversampling proportion [6]. The capacity of low pass separating and down testing can be done utilizing an averaging circuit. The exchange capacity of the averaging circuit is given by condition (1.1). It sets up a connection between the information and yield capacities (1.1)

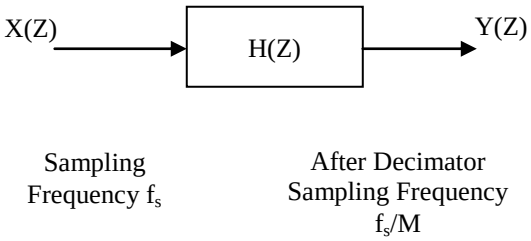

Fig. 1: Block Diagram of Decimator

$$H(Z) = \frac{X(Z)}{Y(Z)} = \frac{1}{M}\sum_{x=0}^{M-1} Z^{-x} \qquad (1)$$

"Up sampling" is the way toward embeddings zero-esteemed examples between unique examples to expand the examining rate. (This is classified "zero-stuffing".) Up testing adds to the first flag undesired ghastly pictures which are fixated on products [7] of the first inspecting rate.

"Introduction", in the DSP sense, is the procedure of up-examining pursued by sifting. (The separating evacuates the undesired phantom pictures.) As a straight procedure, the DSP feeling of insertion is to some degree not the same as the "math" feeling of addition, yet the outcome is reasonably comparable: to make "in the middle of" tests from the first examples.

The outcome is as though you had quite recently initially tested your flag at the higher rate. Expanding the inspecting recurrence use interpolator

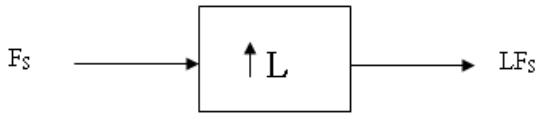

Fig. 2: Interpolation with factor L

Since addition depends on zero-stuffing you can just interject by number components; you can't insert by fragmentary variables. (Be that as it may, you can join insertion and annihilation to accomplish a general sane factor, for instance, 4/5 Up-examining adds undesired phantom pictures to the flag at products of the firstinspecting rate, so except if you expel those by separating, the up-tested flag [7] isn't equivalent to the first: it's contorted.

III. PROPOSED STRUCTURE

In this work the design of a decimation filter is presented for integrating with an existing designed modulator to form a complete sigma-delta ADC. We use multi-organize destruction channel which implies the single pulverization channel is supplanted by fell channels. In this part, we will discuss the channel engineering utilized in this work, including their structures, qualities and downsides. The initial phase in structuring an obliteration channel is to choose which sorts of channels will be utilized and where demolition will happen. This section investigates the issues associated with picking channel design for a listening device application. The general intensity of a few designs is analyzed, bringing about the three-arrange engineering that is picked to actualize this channel.

A typical need in gadgets and DSP is to confine a restricted band of frequencies from a more extensive data transmission flag. Narrowband channels rather catch just a little piece of the range. They are said to have a thin band-pass. The band-pass is basically the amount of the range the channel permits to pass. This is typically estimated in nanometers. Limited band channel comprises of decimator, restricted band and interpolator.

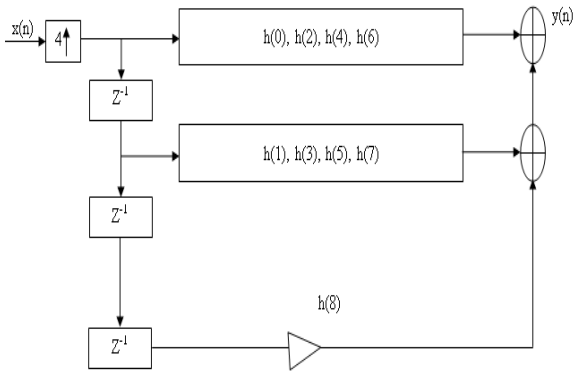

Fig. 3: Interpolator structure with filter order N3=9 and L=4

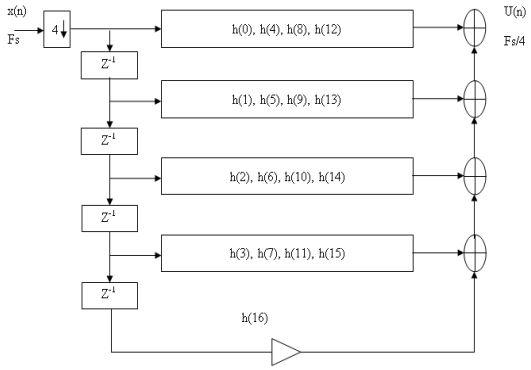

Fig. 4: Decimator structure with filter order N1=17 and M=4

A few applications might have the capacity to endure that; for instance, if the pictures get expelled later by a simple channel, yet in many applications you should evacuate the undesired pictures through advanced sifting.

Along these lines, introduction is undeniably increasingly normal [8] that up-inspecting alone.

Table 1: Theoretical Analysis of Direct Method and Multi-rate Approach for Different Filter Coefficient and Sampling Frequency

Author	***Sampling***		***Filter Coefficient***	***Multiplier***	***Adder***	***Register***	***Cycle Period***
Direct Method	1		08	08	07	07	$08T_S$
	1		09	09	08	08	$09\ T_S$
	1		17	17	16	16	$17\ T_S$
	1		38	38	37	37	$38\ T_S$
	F_S=150Hz		150	150	149	149	$150\ T_S$
Multi-rate Approach	Decimator	2	09	09	08	08	$09\ T_S$
		4	17	17	16	16	$17\ T_S$
	NBF	2	75	75	74	74	$75\ T_S$
		4	38	38	37	37	$38\ T_S$
	Interpolator	2	05	05	04	04	$05\ T_S$
		4	09	09	08	08	$09\ T_S$

IV. SIMULATION RESULT

The proposed architecture has very low hardware complexity compared to direct approach based structures, because direct method requires more multiplier compare to proposed architecture. In the proposed architecture, calculate the decimator and interpolator structure for design a narrow band filter.

Table 2: Comparison Result for Previous and Proposed Approach for N=5

	Previous Approach	Proposed Approach
Number of Slice	45	34
Number of Flip Flops	39	32
No. of Slice LUTs	63	57
MCPD (ns)	17.564	14.352

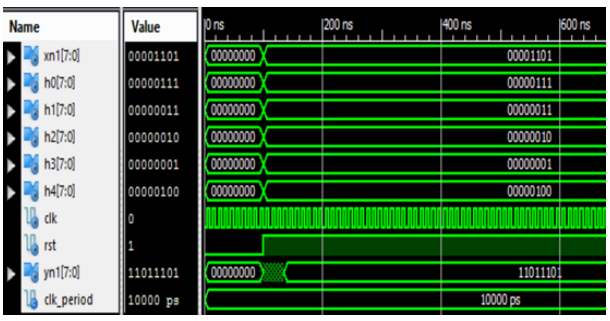

Fig. 5: Output Test Bench Waveform of Narrow Band Filter (Filter Coefficient N=5)

Table 1 shows the theoretical analysis of direct method & multi-rate approach for different filter coefficient and sampling frequency. Table 2 shows cell usage for the Comparison of Performance of the Proposed Implementation and the Existing Implementation of Narrow Band Filter.

The design as were discussed in figure 3 and figure 4 were implemented using VHDL and then were tested on model sim to determine the number of slice and maximum high frequency. In figure 5, figure 6 and figure 6 have shown the output waveform of narrow band filter and chat between filter order and slices. In figure 6, compare the result between numbers of slice and filter order. Increase the filter order also increase the number of slice shown if figure 6.

Table 3: Comparison Result for Previous and Proposed Approach for N=9

	Previous Approach	Proposed Approach
Number of Slice	74	66
Number of Flip Flops	71	64
No. of Slice LUTs	141	113
MCPD (ns)	22.432	17.085

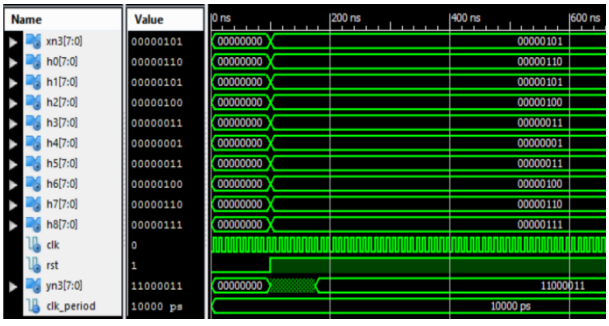

Fig. 6: Output Waveform of 9_tap Narrow Band Filter

V. CONCLUSION

The narrowband filter is realized in FIR filter. Based on the direct approach, the filter requires 150 filter coefficients to meet the desired frequency response. To implement such a large order FIR filter in hardware involves large resources and sometime difficult to implement in resource constrained application. Keeping this in view, we have used Multirate approach to design the narrowband filter. We have used down sampling factor 2 and 4 for this purpose and found that, down sampling factor 4 requires significantly less filter constants than 2. To implement the narrowband filter, we therefore chosen down sampling factor 4 and designed the decimator, interpolator and narrowband filter. The total number of filter coefficients required to realize the decimator, interpolator and the narrowband filter 64 which is almost 58% less than the direct method.

REFERENCES

[1] Basant K. Mohanty, Pramod Kumar Meher, and Sujit K. Patel, "LUT Optimization for Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE 2015.

[2] Ming Liu, Ming-Jiang Wang and Bo-Yang Song, "An efficient architecture of the sign-error LMS adaptive filter", Solid-State and Integrated Circuit Technology (ICSICT), 13th IEEE International Conference on, IEEE 2016.

[3] Ch. Sravani and U. V RatnaKumari, "Implementation fixed-point Least Mean Square adaptive filter for low area and delay", Signal Processing, Communication, Power and Embedded System (SCOPES), International Conference on, IEEE 2016.

[4] Sireesha N, K. Chithra and Tata Sudhakar, "Performance analysis of linear recursive least squares adaptive filter to mitigate multipath effect", Ocean Electronics (SYMPOL), 2015 International Symposium on, IEEE 2015.

[5] Raymond Lee, Mohammed A.S. Khalid and Esam Abdel-Raheem, "Configurable hardware implementation of a pipelined DNLMS adaptive filter", Microelectronics (ICM), 26th International Conference on, IEEE 2014.

[6] P. Priya and P. Babu, "An efficient architecture for the adaptive filter using delayed LMS algorithm", Information Communication and Embedded Systems (ICICES), 2014 International Conference on, IEEE 2014.

[7] S. Y. Park and P. K. Meher, "Low-power, high-throughput, and low-area adaptive FIR filter based on distributed arithmetic," IEEE Trans. Circuits System- II, Exp. Briefs, Vol. 60, No. 6, pp. 346–350, Jun. 2013.

[8] B. K. Mohanty and P. K. Meher, "A high-performance energy-efficient architecture for FIR adaptive filter based on new distributed arithmetic formulation of block LMS algorithm," IEEE Trans. Signal Process.,vol. 61, no. 4, pp. 921–932, Feb. 2013.

[9] Azadeh Safari and Yinan Kong "Four tap Daubechies filter banks based on RNS", IEEE International Conference on Image Processing, Signal and System, 2012.

[10] M. Chuang and C. Wang, "Reversible sequential element designs", *Proceedings of the IEEE Asia and South Pacific Design Automation Conference*, pp. 420-425, 2007.

[11] G. Challa Ram and D.Sudha Rani, "Area Efficient Modified Vedic Multiplier", 2016 International Conference on Circuit, Power and Computing Technologies(ICCPCT).

[12] S. P. Pohokar, R. S. Sisal, K. M. Gaikwad, M. M. Patil and RushikeshBorse, "Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics", International Conference on Industrial Instrumentation and Control (ICIC) College of Engineering Pune, India, PP. No. 01-06, 2015.