Design of FIR Filter using Brent Kung Adder to reduce Minimum Clock Period(MCP)

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Abstract – The Finite Impulse Response(FIR) filter is used in many digital signal processing systems, in order to reduce Minimum Clock Period, area and delay. FIR Filter has widespread application in signal processing such as image processing, high speed communication systems, biomedical signal processing, noise elimination and many more. In this paper, Finite Impulse Response(FIR) Filter is designed using Brent Kung Adder (BKA) to reduce Minimum Clock Period(MCP). The proposed 32-bit Brent Kung Adder has been improved by splitting into four phases. Brent Kung Adder is used because it processes signal in a parallel manner. It increases the speed and to reduce complexity of the Finite Impulse Response(FIR) filter. Ripple Carry Adder(RCA) used in previous work has drawback in delay as next process has to wait until the all carry generated along the way. Propose Brent Kung Adder plays an important role where speed and delay need not to compromise while designing circuit. In this work logical element is changed of finite impulse response filter. Delay performance is compared between Ripple Carry Adder and Brent Kung Adder. To examine proposed logic a digital filter of length 8 and 16 has implemented and synthesized in Xilinx 13.1 ISE design suite.

Keywords: Retiming, Finite Impulse Response, Brent Kung Adder, Fixed-point arithmetic, Ripple Carry Adder, Minimum Clock Period(MCP).

I. INTRODUCTION

Digital filters are very important part of DSP. In fact their extraordinary performance is one of the key reasons that DSP has become so popular. Filters have two uses: signal separation and signal restoration. Signal separation is needed when the signal has been contaminated with interference, noise or other signals.

Finite Impulse Response (FIR) filters are widely used in Digital Signal Processing (DSP) applications due to their stability and linear-phase property. In today scenario, low power consumption and less area are the most important parameter for the fabrication of DSP systems and high performance systems. The implementation of an FIR filter requires three basic building blocks. They are Multiplication, Addition and Signal delay. The exiting adder is ripple carry adder and the multiplier is Wallace tree multiplier, both take more area and delay. The Input samples and coefficient to be of L-bit words, and the product word to be of 2L bits [1]. We change the logical element of Finite Impulse Response Filter. In previous work, architecture of FIR filter change using Retiming and presented connected component timing model to reduce Minimum clock period, Area and Area delay product(ADP) of design. They used ripple carry adder and Wallace tree multiplier in finite impulse response filter design. In our work, Brent Kung Adder replacing Ripple Carry Adder in Finite impulse response filter.

FIR Filter:

The FIR means “Finite Impulse Response”. The FIR filters are of the non-recursive type whereby the present output sample depends on the present input sample and previous input sample. Recursive is a type of filter which reuses one or more of its outputs as an input. In signal processing, a FIR filter is a filter whose impulse response (or response to any finite length input) is of finite duration because it settles to zero in finite time. This FIR filter’s ability to provide stable linear- phase behaviour has made it gain acceptance in wide kind of signal processing applications. Since FIR filters have a capability of no phase distortion, they are considered as important.

The frequency response of FIR filter is based on the value of coefficients or taps. The impulse response of a FIR digital filter is of finite duration[14]. The below difference equation describes the FIR filter with length N, input x(n) and output y(n). where, h(k) is the set of filter coefficients.

$$y(n)= \sum_{k=0}^{N-1} h(k)x(n-k) \quad \text{Difference equation}$$

where y(n) is output, h(k) coefficient and x(n) input.

The design of the FIR filter is shown in Figure 1.1.The implementation of an FIR requires three basic building blocks: Multiplication, Addition and Signal delay. The number of stages is depending upon the length of the filter. And also this is directly proportional to the tap [17].

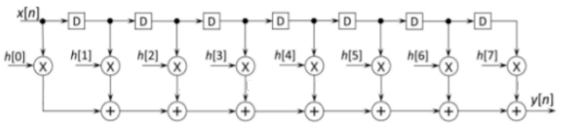

Figure1.1: The DFG of FIR Filter of length N=8

Brent Kung Adder:

Brent-Kung Adder is a very well-known logarithmic adder architecture that gives an optimal number of stages from

input to all outputs but with asymmetric loading on all intermediate stages. It is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in brent kung adders. But the gate level depth of Brent-Kung adders is 0 (log2(n)), so the speed is lower. Brent-Kung adder is a parallel prefix adder which gives fast result, much simpler to built, minimum number of nodes and save power, it is considered to be one of the most flexible adders.

The execution speed of Brent Kung is higher as compare to other. In parallel adders the critical path is decided by computation of the carry from LSB adder to the MSB adder, therefore efforts are in reducing the critical path for the carry to reach the MSB.

It consist three steps:

1. Pre- processing stage

2. Carry generation network

3. Post processing stage

Pre- processing stage

In this stage, Generate and Propagate signal are computed for the N-bit input values to the adder. Signals are generated and propagate in each pair of inputs A and B. These signals are given by the following equations:

$$P_i = A_i \text{ xor } B_i$$

$$G_i = A_i \text{ and } B_i$$

Carry generation network

Carry generation network is a middle stage of Brent Kung adder in which signal from the first stage will proceed with the next stage. Implementation of these operations is carried out in parallel, and then signal are carried out and converted into small pieces.

$$G = (g2 \mid (g1\&p2));$$

$$P = p1\&p2$$

Post processing Stage

This is the Final Stage in architecture is the sum generation stage, where each bit are added in the parallel form and they are summed up together up using XOR gate. These is the last stage where, carry bits produced from second stage given next stage and that last stage is known as post processing .

$$S_i = P_i \oplus C_{i-1} \qquad \text{where } C_{i-1} = P_i . C_{in} + G_i$$

In carry generation network, the first row the prefixes are computed for 2-bit groups. These in turn are used to find the prefixes for 4-bit groups, and then these are used to compute prefixes for 8-bit groups and so forth. And these prefixes are fan back down to calculate the carry in of each bit.

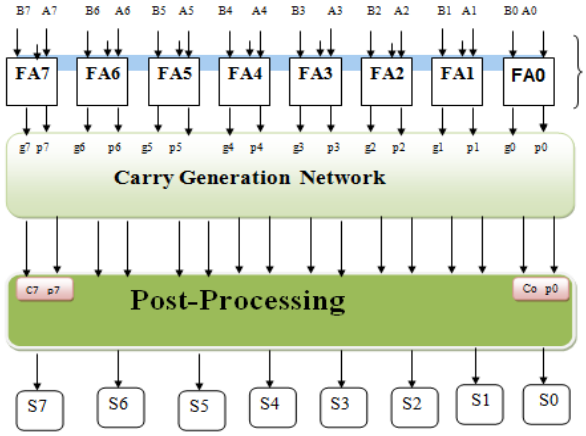

Figure 1.2: 8-Bit Brent Kung Adder

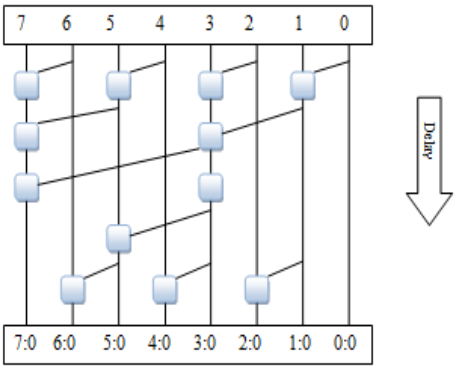

Figure 1.3: 8-Bit Carry generation network

Ripple Carry Adder:

Ripple Carry Adder is constructed by cascading full adder blocks in series. A Ripple Carry Adder is a logic circuit in which the carry out of one stage fed directly to the carry in of the next stage. It is called Ripple Carry Adder because each carry bit gets rippled into the next stage. It gives the most compact design. This adder is used in previous work, which is take longer computation time.But the major drawback turns out to be the delay in obtaining the output. Each stage is dependent on the carry produced by the previous stage. This causes a major delay as we have to wait until the carries are generated along the way.

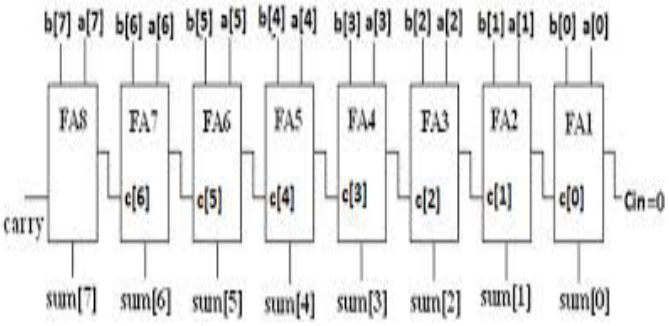

Figure1.4 8-Bit Ripple Carry Adder

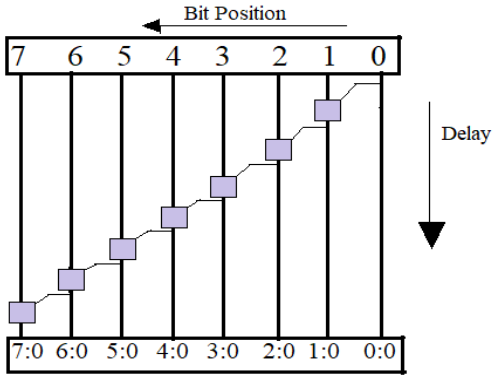

Figure 1.5: 8-Bit Carry network of RCA

Retiming:

Retiming is a transformation technique used to change the location of a delay elements in a circuit without affecting the characteristics of the circuit[11] [12]. Leiserson and Saxe provided the first formulation and theoretical solution to this problem in 1983, although their later has the most complete overview of this work. This technique has no of applications in designing and optimization of circuits e.g. clock period is reduced, total number of registers used in circuit can be reduced, required power to run the circuit can be decreased. The central objective of retiming is to find a circuit with the minimum number of registers for a specified clock period. There are two common variants of this theme; minimizing the clock period without regard to the number of registers in the final circuit or minimizing the number of registers in the final circuit with no constraints on the clock period. The technique used for dividing a normal data flow graph into sub graphs can be called Cutset Retiming. This can be implemented by changing the position of certain no of delays to or from incoming and outgoing edges of the sub graphs. This can be effectively used in architectural level of designing a digital system for deduction of period of clock.

As a means of motivating and introducing the concept of retiming, consider a simple example in Figure 1.6.

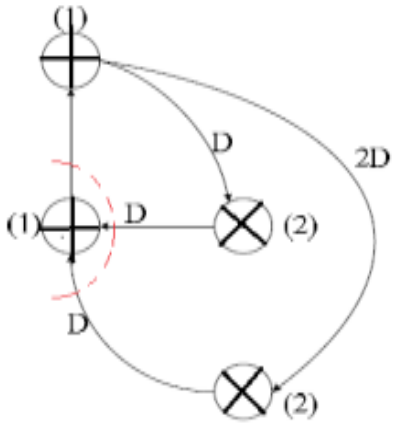

Figure 1.6 A Simple Circuit

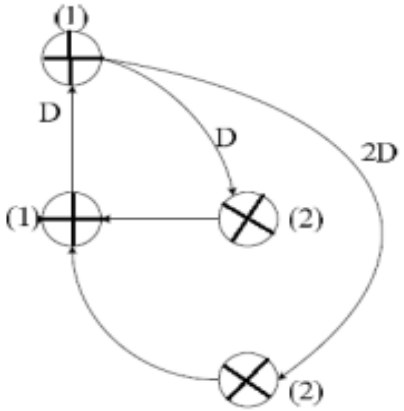

Figure 1.7 Retiming for Minimum Register

Retiming can either shift the exiting register in the design or can be followed by pipelining, where the designer places a number of register on a cutest line and then applies a retiming conversion to place these registers at appropriate edge to minimize the critical path while keeping all the other objectives as the resulting purpose.

II. PROBLEM DESCRIPTION

In Ripple Carry Adder(RCA), delay increases linearly with the bit length. It takes longer computation time. RCA is not very efficient when large bit numbers are used. The minimal period retiming problem, that is, moving the flip-flop to minimize the clock period that is decided by the longest delay between two consecutive flip-flops. The minimal period retiming problem was always solved through a sequence of fixed period retiming problems each of which checks whether a given clock is feasible. A binary search is used to find the smallest feasible period. In cases when the periods may change continuously, the binary search approach only gives a fully polynomial-time approximation. The running time is dependent on the required precisions.

III. PROPOSED METHODOLOGY

In this research examination work minimum clock period measured optimized retiming of FIR circuit using Brent Kung Adder for filter length 8 and 16 has proposed and implemented on Xilinx13.1 design suite.

Steps of implementation of a proposed design using Xilinx ISE in hardware description language. The steps involved in implementation of proposed design are briefed as follows:

Step 1: Create New Project: Using Xilinx ISE design suite create a new project in project navigator and select target device to implement project.

Step 2: Write program for proposed design in Verilog HDL (hardware description language) specify IO ports. Using mixed modeling style of hardware design describe behavioral and structural design of proposed model. To

model a parallel prefix BK adder functions for all three stages are discussed in equation.

Step 3: Save and Check Syntax: Save written program for proposed design and check for syntax error.

Step 4: Synthesis: Run behavioral synthesis to implement behavior of proposed design in to hardware and generate Xst file and Netlist file.

Step 5: View RTL schematic and technology schematic of implemented design in Xilinx to examine and compare with model design to verify.

Step 6: Verification: To verify proposed design testbench are created in UVM . To verify using testbench, random simulates are provided and results are examined and compared with expected outcome or standard outcome. The testbench verification shows that proposed design shows expected behavioral functionally defined by user.

Step 7: View synthesis summary to examine device utilization and critical delay in circuit. Compare results with existing previous work with respect to LUTs, FF, and delay in ns.

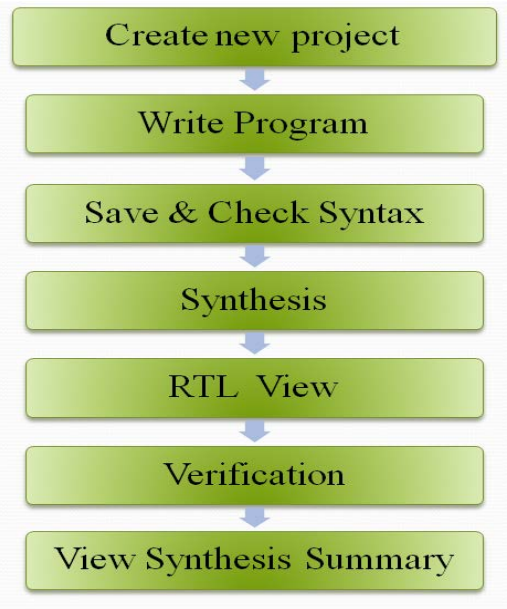

Fig. 2.1 shows the RTL schematic of implementation of proposed design of digital filter of length 8 in Xilinx.

The Figure 2.1 is the top module of proposed design having 12 input output pins. The input width is (15:0) 16 bit, filter coefficient is (15:0) 16bit and output is (31:0) 32 bit. There are 8 input vectors in proposed design with width bit are h0, h1, h2, h3, h4, h5, h6, h7. One is a clock used to provide clock to the circuit and another one is reset pin to reset operation in its base state.

Here D-flip flop is a unit delay, which provide a one sample signal delay. A sample value is stored in a memory slot for one sample clock cycle, and then made available as input to the next processing stage. An M-unit delay requires M memory cells configured as a shift register. We used 16-Bit input and it work on positive edge.

Our Filter consists of 8 adder and 9 multiplier. The duration of impulse response is finite which range from 0 to 7. The impulse response of an 7^{th} order FIR filter.

We used (16*16) Multiplier using Add and shift method, which gives 32-bit output and 32-bit(8*4) Brent kung adder.

RTL schematic of sub-modules of proposed design module has shows in Fig. 2.2 & Fig. 2.3 RTL Schematic of Sub-Modules.

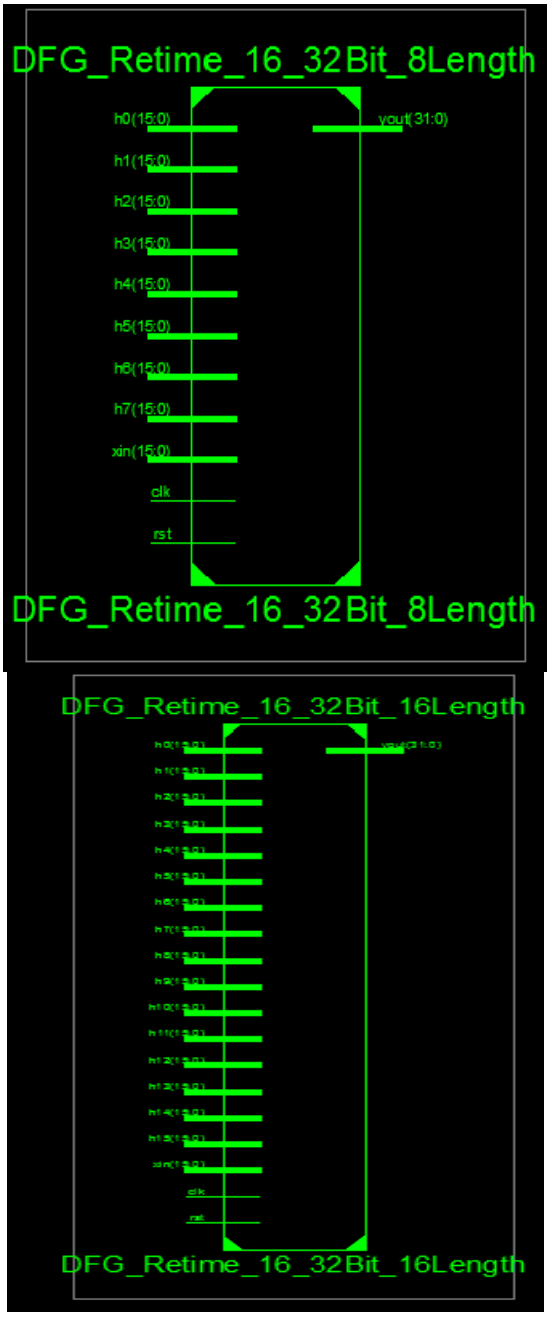

Fig.2.1 RTL Schematic of Top Module Filter length 8 and 16

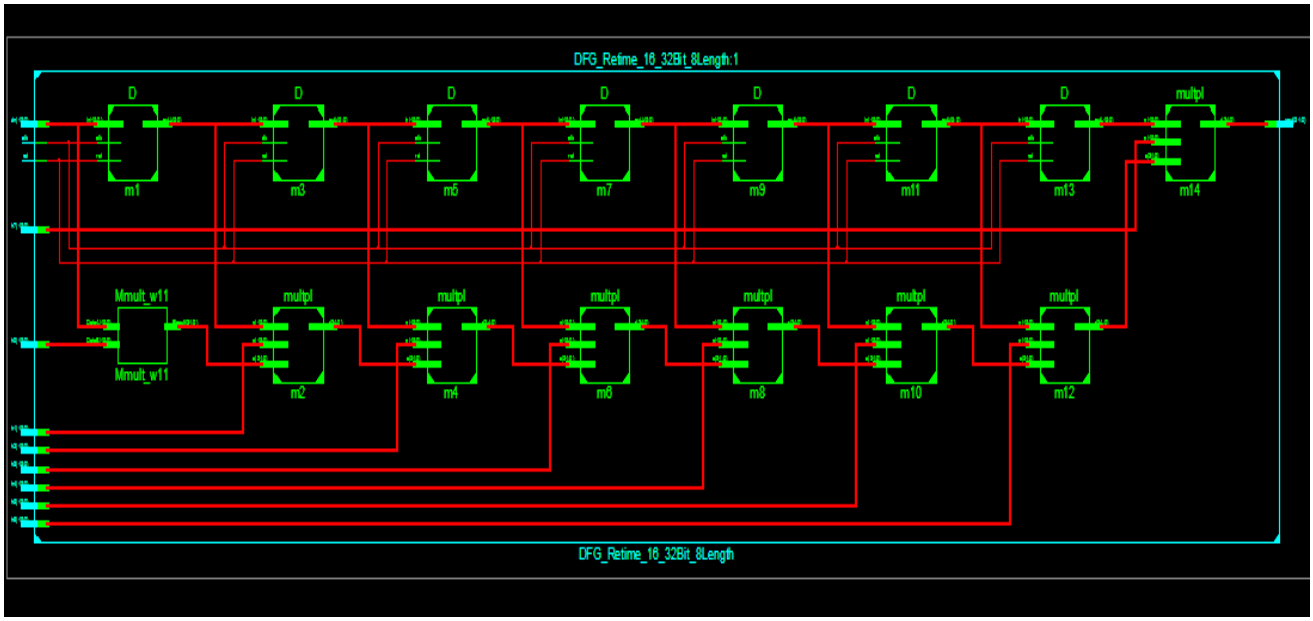

Figure 2.2 RTL Schematic of Sub- Modules Filter length 8

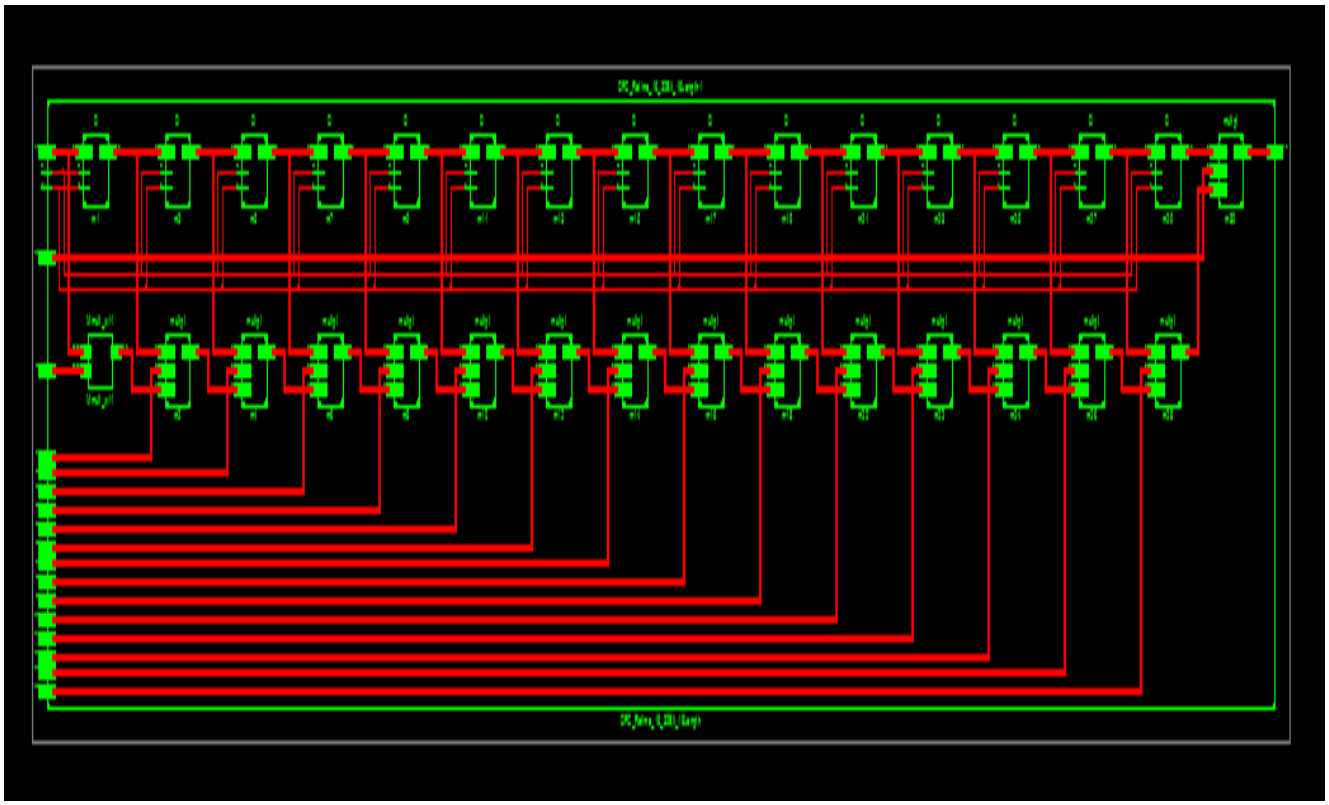

Figure 2.3 RTL Schematic of Sub-modules Filter length 16

IV. SIMULATION RESULTS

In this work implemented a program that minimizes the MCP of the Fir Filter circuit using Brent Kung Adder. The HDL program is designed and implemented in Xilinx ISE design suite and synthesized in this examination.

Table-1 shows the comparative analysis of proposed work with existing work for 8- bit RC Adder used in previous work and BK Adder used in proposed work in terms of delay. BK Adder shows better performance in terms of delay, Slice LUTs and Flip-Flop pairs as compared to previous RC Adder work.

Table-1 Comparison of Ripple Carry Adder and Brent Kung Adder

PARAMETER	**RC ADDER**	**BK ADDER**
Delay	8.411ns	5.725ns
Slice LUTs	12	8
Flip Flop pairs	12	8

Fig. 3.1 and 3.2 shows the synthesis screen shots software synthesis of proposed design of digital filter of length 8 in

Xilinx device utilization summary of proposed architecture for Filter length 8 and 16. Synthesis screen shows the device utilization summary of proposed work based on the number of slice registers, number of slice LUTs used 3567, number of bonded IOBs and number of BUFG/BUFGCTRLs used.

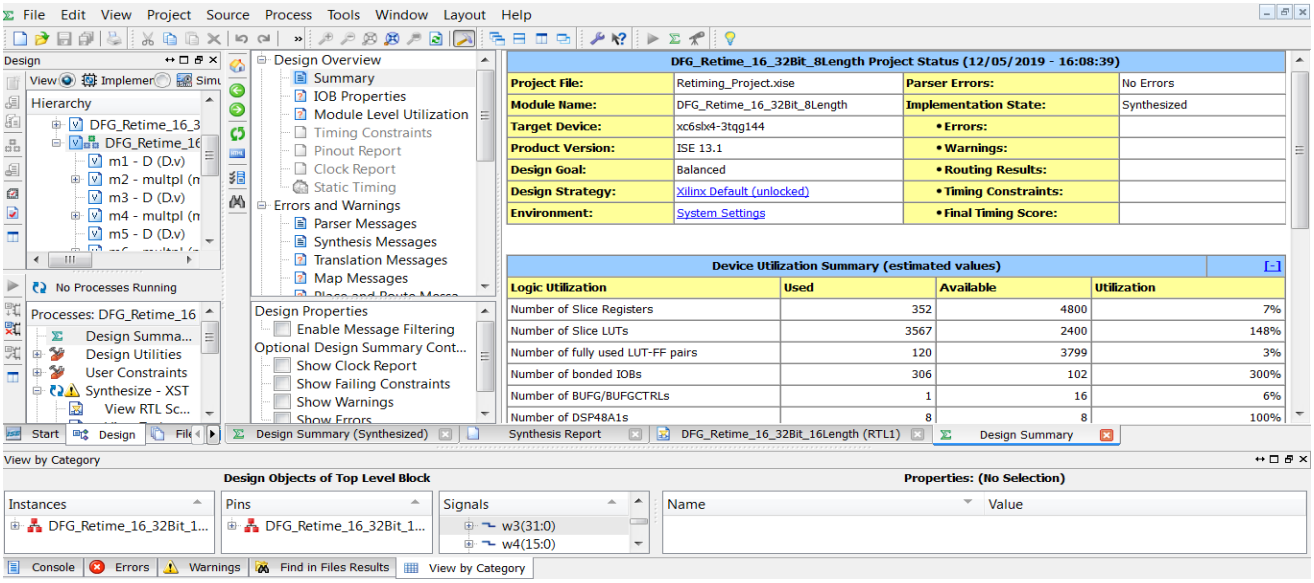

Fig. 3.1 Screen Shots of Summary of Proposed Architecture for FIR Filter of length 8.

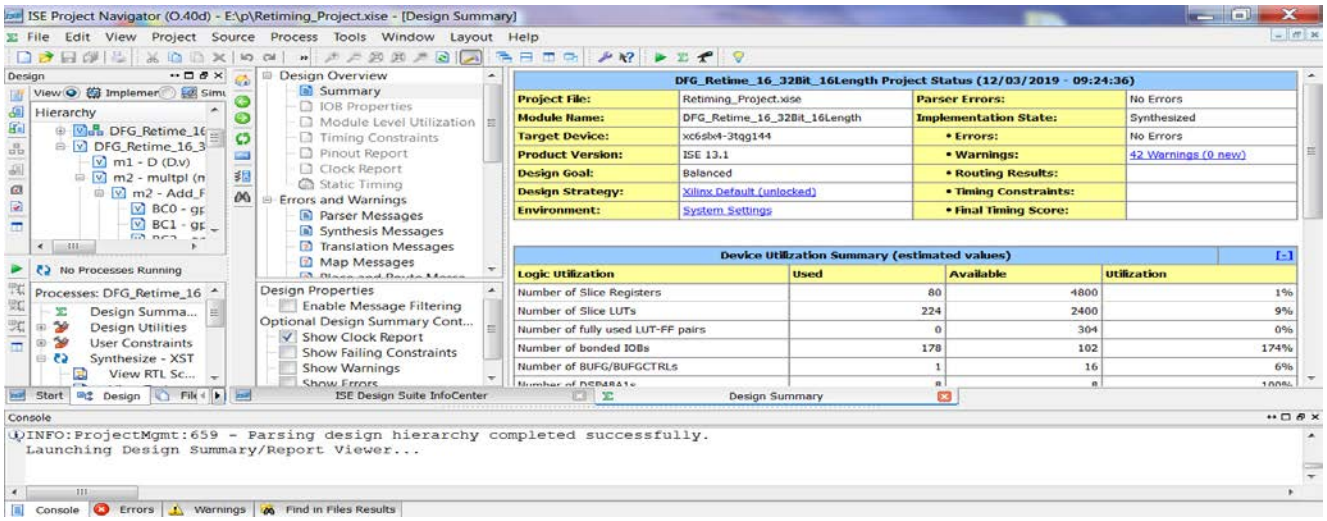

Fig. 3.2 Screen Shots of Summary of Proposed Architecture for FIR Filter of length 16.

Timing summary of proposed architecture to examine MCP is shown in Fig. 3.3 filter length considered for to implement and examine is 8 and MCP computed is 1.212 ns and Fig. 3.4 filter length 16 MCP is 1.246 which is better than previous work. Table: 2 shows the performance comparison of proposed work with existing base work for the FIR filter of length 8 and 16.

Table:2 Performance Comparison

Parameter	***Previous [1] FIR Retiming***	***Proposed (our) FIR using BK Adder***
Filter Length	8	8
Minimum Clock Period	3.39ns	**1.212 ns**

Parameter	***Previous [1] FIR Retiming***	***Proposed (our) FIR using BK Adder***
Filter Length	16	16
Minimum Clock Period	3.39ns	**1.246 ns**

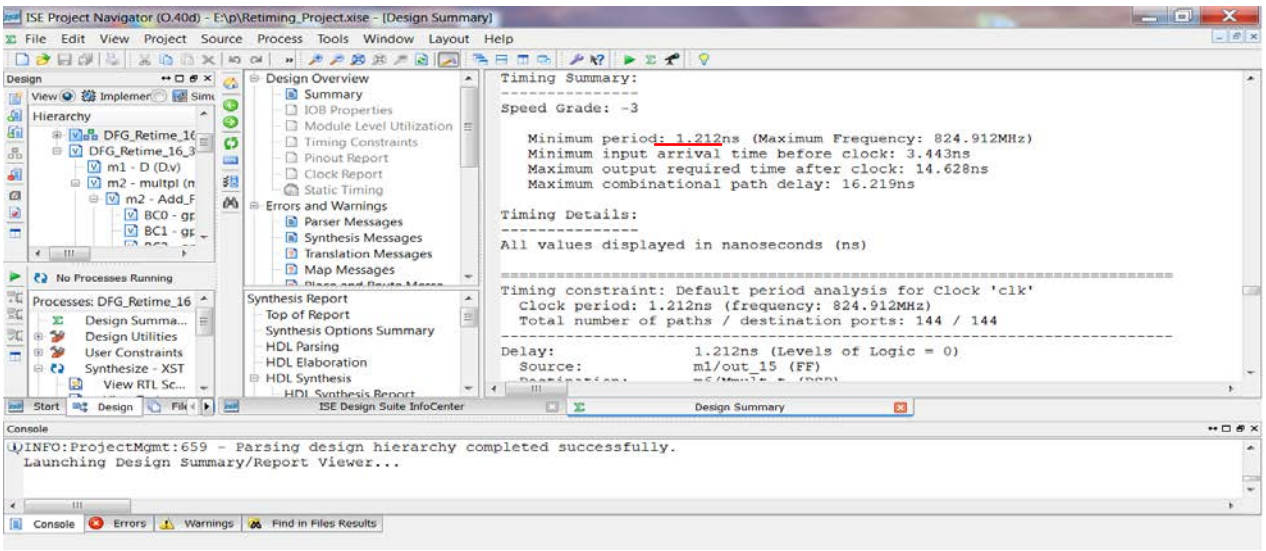

Fig. 3.3 MCP of proposed architecture for Filter length 8.

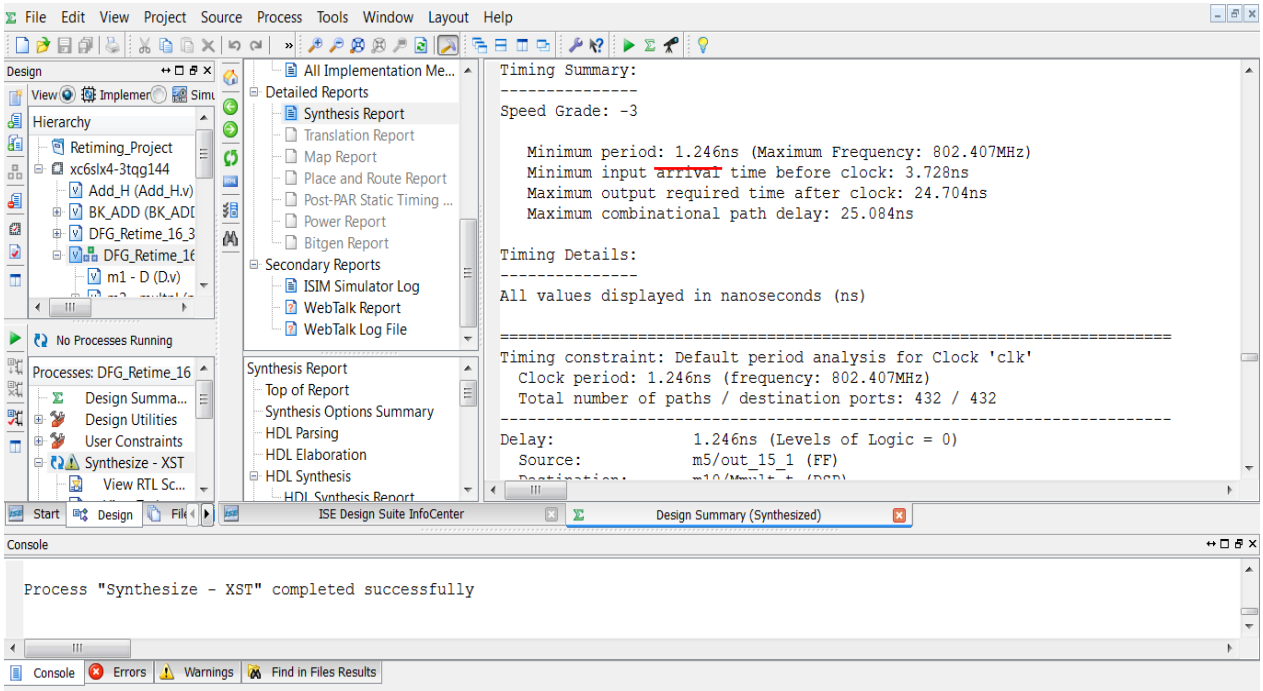

Fig. 3.4 MCP of proposed architecture for Filter length 16.

V. CONCLUSION

In this work an FIR filter designed by using Brent kung adder to increase the speed and to reduce complexity. Brent kung adder is used because it processes in a parallel manner and the output can be easily obtained. By doing so we are increasing the speed of the process. This work presented a MCP optimized of Finite Impulse Response Filter using Brent Kung Adder considering seamless signal propagation in circuits, which provides a simple way to obtain adequately precise estimate of propagation delays across different paths in a DFG. Minimum Clock Period is compared between for Filter Length 8 and 16. Comparison shows that significant improvement in MCP. Delay element is also compared between Ripple Carry Adder and Brent Kung Adder, which shows that Brent kung adder is low delay than Ripple Carry Adder.

This technique of fixed points circuits can be extended to floating point circuits. In FIR Filter, Adder and Multiplier can be change.

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