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A Brief Study on Retiming of Digital Circuits

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Abstract - In signal processing applications the time basic areas are iterative and recursive and requires different streamlining methods for execution improvement. A large portion of these applications require every cycle to be executed under a particular time limitation related with the information input rate. Utilizing improvement methods like retiming, we accomplish the coveted execution. Advanced channels are the most widely recognized squares in signal processing applications and they can be spoken to by synchronous information stream charts (DFGs). Applying retiming procedures on the synchronous information stream charts brings about acquiring rapid advanced circuits. Retiming is the way toward modifying the capacity components in the circuit to diminish the process duration without changing its usefulness. In this research work, a solitary streamlining condition is created for retiming the DSP channel squares utilizing cutset and clock period minimization strategies. Cutset retiming is exceptionally utilized for channels intended for single processor frameworks. An upgraded advanced channel circuit is gotten subsequent to retiming from plan improvement condition. Likewise, the HDL(Hardware Description Language) code of the streamlined channel circuit is consequently created and micro architectural advancements like use of parallel prefix tree adders, supply voltage scaling are done at auxiliary level of the circuit which still upgrades the channel plan execution.

Keywords: Cutset retiming, digital signal processing (DSP) hardware, fixed-point arithmetic, retiming.

I. INTRODUCTION

Digital filters are very important part of DSP. In fact their extraordinary performance is one of the key reasons that DSP has become so popular. Filters have two uses: signal separation and signal restoration. Signal separation is needed when the signal has been contaminated with interference, noise or other signals.

Finite Impulse Response (FIR) filters are widely used in Digital Signal Processing (DSP) applications due to their stability and linear-phase property. In today scenario, low power consumption and less area are the most important parameter for the fabrication of DSP systems and high performance systems. The implementation of an FIR filter requires three basic building blocks. They are Multiplication, Addition and Signal delay. The exiting adder is ripple carry adder and the multiplier is Wallace tree multiplier, both take more area and delay. The Input samples and coefficient to be of L-bit words, and the product word to be of 2L bits [1]. We change the logical element of Finite Impulse Response Filter. In previous work, architecture of FIR filter change using Retiming and presented connected component timing model to reduce Minimum clock period, Area and Area delay product(ADP) of design. They used ripple carry adder and Wallace tree multiplier in finite impulse response filter design. In our work, Brent Kung Adder replacing Ripple Carry Adder in Finite impulse response filter.

FIR Filter:

The FIR means “Finite Impulse Response”. The FIR filters are of the non-recursive type whereby the present output sample depends on the present input sample and previous input sample. Recursive is a type of filter which reuses one or more of its outputs as an input. In signal processing, a FIR filter is a filter whose impulse response (or response to any finite length input) is of finite duration because it settles to zero in finite time. This FIR filter’s ability to provide stable linear- phase behaviour has made it gain acceptance in wide kind of signal processing applications. Since FIR filters have a capability of no phase distortion, they are considered as important.

The frequency response of FIR filter is based on the value of coefficients or taps. The impulse response of a FIR digital filter is of finite duration[14]. The below difference equation describes the FIR filter with length N, input x(n) and output y(n). where, h(k) is the set of filter coefficients.

$$y(n)= \sum_{k=0}^{N-1} h(k)x(n-k) \quad \text{Difference equation}$$

where y(n) is output, h(k) coefficient and x(n) input.

The design of the FIR filter is shown in Figure 1.1.The implementation of an FIR requires three basic building blocks: Multiplication, Addition and Signal delay. The number of stages is depending upon the length of the filter. And also this is directly proportional to the tap [17].

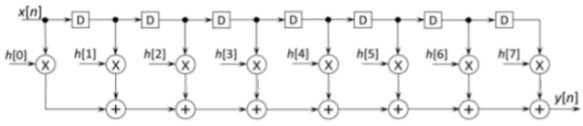

Figure1.1: The DFG of FIR Filter of length N=8

Brent Kung Adder:

Brent-Kung Adder is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. It is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are

based on the use of generate and propagate signals. The cost and wiring complexity is less in brent kung adders. But the gate level depth of Brent-Kung adders is 0 (log2(n)), so the speed is lower. Brent-Kung adder is a parallel prefix adder which gives fast result, much simpler to built, minimum number of nodes and save power, it is considered to be one of the most flexible adders.

The execution speed of Brent Kung is higher as compare to other. In parallel adders the critical path is decided by computation of the carry from LSB adder to the MSB adder, therefore efforts are in reducing the critical path for the carry to reach the MSB.

It consist three steps:

1. Pre- processing stage
2. Carry generation network
3. Post processing stage

Pre- processing stage

In this stage, Generate and Propagate signal are computed for the N-bit input values to the adder. Signals are generated and propagate in each pair of inputs A and B. These signals are given by the following equations:

$$P_i = A_i \text{ xor } B_i$$

$$G_i = A_i \text{ and } B_i$$

Carry generation network

Carry generation network is a middle stage of Brent Kung adder in which signal from the first stage will proceed with the next stage. Implementation of these operations is carried out in parallel, and then signal are carried out and converted into small pieces.

G= (g2 | (g1&p2));

P = p1&p2

Post processing Stage

This is the Final Stage in architecture is the sum generation stage, where each bit are added in the parallel form and they are summed up together up using XOR gate. These is the last stage where, carry bits produced from second stage given next stage and that last stage is known as post processing .

$$S_i = P_i \oplus C_{i-1} \qquad \text{where } C_{i-1} = P_i . C_{in} + G_i$$

In carry generation network, the first row the prefixes are computed for 2-bit groups. These in turn are used to find the prefixes for 4-bit groups, and then these are used to compute prefixes for 8-bit groups and so forth. And these prefixes are fan back down to calculate the carry in of each bit.

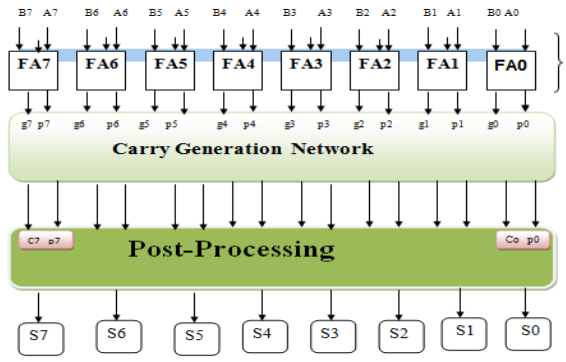

Figure 1.2: 8-Bit Brent Kung Adder

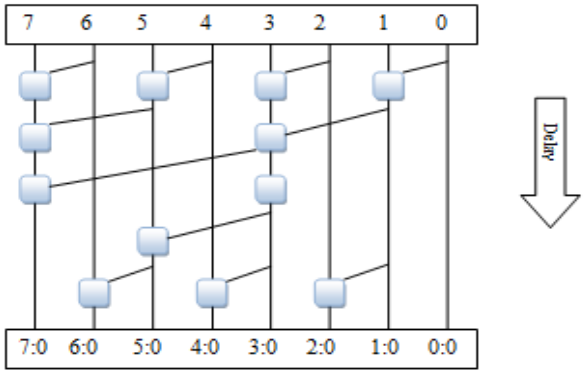

Figure 1.3: 8-Bit Carry generation network

Ripple Carry Adder:

Ripple Carry Adder is constructed by cascading full adder blocks in series. A Ripple Carry Adder is a logic circuit in which the carry out of one stage fed directly to the carry in of the next stage. It is called Ripple Carry Adder because each carry bit gets rippled into the next stage. It gives the most compact design.

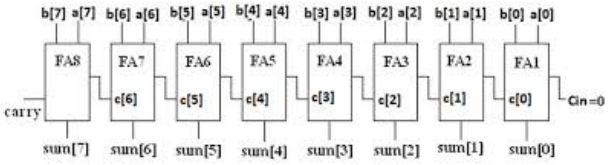

Figure1.4 8-Bit Ripple Carry Adder

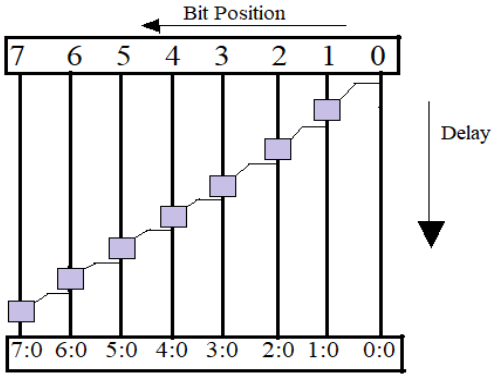

Figure 1.5: 8-Bit Carry network of RCA

This adder is used in previous work, which is take longer computation time.But the major drawback turns out to be the delay in obtaining the output. Each stage is dependent on the carry produced by the previous stage. This causes a major delay as we have to wait until the carries are generated along the way.

Retiming:

Retiming is a transformation technique used to change the location of a delay elements in a circuit without affecting the characteristics of the circuit[11] [12]. Leiserson and Saxe provided the first formulation and theoretical solution to this problem in 1983, although their later has the most complete overview of this work. This technique has no of applications in designing and optimization of circuits e.g. clock period is reduced, total number of registers used in circuit can be reduced, required power to run the circuit can be decreased. The central objective of retiming is to find a circuit with the minimum number of registers for a specified clock period. There are two common variants of this theme; minimizing the clock period without regard to the number of registers in the final circuit or minimizing the number of registers in the final circuit with no constraints on the clock period. The technique used for dividing a normal data flow graph into sub graphs can be called Cutset Retiming. This can be implemented by changing the position of certain no of delays to or from incoming and outgoing edges of the sub graphs. This can be effectively used in architectural level of designing a digital system for deduction of period of clock.

As a means of motivating and introducing the concept of retiming, consider a simple example in Figure 1.6.

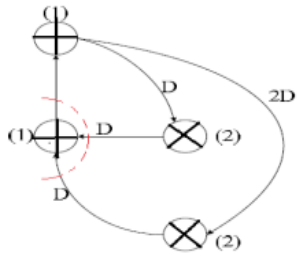

Figure 1.6 A Simple Circuit

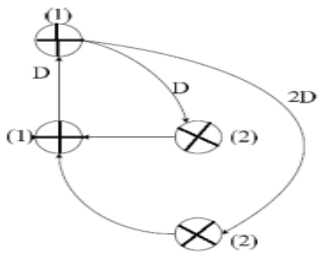

Figure 1.7 Retiming for Minimum Register

Retiming can either shift the exiting register in the design or can be followed by pipelining, where the designer places a number of register on a cutest line and then applies a retiming conversion to place these registers at appropriate edge to minimize the critical path while keeping all the other objectives as the resulting purpose.

II. PROBLEM DESCRIPTION

In Ripple Carry Adder(RCA), delay increases linearly with the bit length. It takes longer computation time. RCA is not very efficient when large bit numbers are used. The minimal period retiming problem, that is, moving the flip-flop to minimize the clock period that is decided by the longest delay between two consecutive flip-flops. The minimal period retiming problem was always solved through a sequence of fixed period retiming problems each of which checks whether a given clock is feasible. A binary search is used to find the smallest feasible period. In cases when the periods may change continuously, the binary search approach only gives a fully polynomial-time approximation. The running time is dependent on the required precisions.

III. LITERATURE REVIEW

P. K. Meher, "On Efficient Retiming of Fixed-Point Circuits[1]," In this research work, Pramod Kumar Mehar proposed the connected component timing model considering seamless signal propagation in combinational circuits. Connected component timing model provides precise estimate of propagation delay(PD) across combinational paths in a DFG , for efficient cutset-retiming in order to reduce the critical path substantially without significant increase in register-complexity and latency. Apart from that, author propose novel node-splitting and node-merging techniques that can be used in combination with the existing retiming methods to achieve reduction of critical path to a fraction that of the original DFG with a small increase in overall register complexity. Flexible and efficient retiming of Finite Impulse Response filters where they achieve reduction of critical path using less pipeline registers. Such a discrete component timing model very often gives much higher estimates of the propagation delays than the actuals particularly when the computations in the DFG nodes correspond to fixed-point arithmetic operations like additions and multiplications. It shows that lower critical path for small filter lengths, but for higher filter lengths the proposed retiming lower critical path.

S. Guo et al., "A low-power 28 Gb/s CDR using artificial lc transmission line technique in 65 nm CMOS[2]," In this research work , S. Guo represented a low-power 28 Gb/s Phase Locked Loop-based clock and data recovery circuit in 65 nm CMOS technology. Clock and Data Recovery circuit monitor transition of the data signal and select an

optimal sample phase for the data at the midpoint between edges. The artificial LC transmission line technique is proposed to be used in the full-rate bang-bang phase detector to reduce the number of D-latches and save power consumption by 42.8% compared with the conventional phase detector design. By using the transmission line technique, the retiming circuit is merged into the phase detector, which further saves power of the data retiming circuit. The compact phase detector with built-in retiming circuit also alleviates the capacitive loading of and saves corresponding power consumed by the clock buffer. In addition, the artificial LC transmission line is proposed to be used in the clock buffer to drive the distributed capacitive loads presented by separate D-latch and save power consumption by 50% compared with the conventional inductive peaking clock buffer. The total power consumption of the Clock and Data Recovery(CDR) is 35 mW from a 1.1 V supply.

N. Kito, K. Takagi and N. Takagi, "Conversion of a CMOS Logic Circuit Design to an RSFQ Design Considering Latching Function of RSFQ Logic Gates[3],” In this paper, Authors proposed method for change a cmos logic circuit to Rapid single flux quantum(RSFQ). This method minimizes the numbers of flipflop. In this conversion, latching function is enable or disabled when each data input terminal of a logic gate has latching function. Its depending on the order of the arrivals of the data pulse and clock pulse.In Rapid single flux quantum(RSFQ) information is stored in the form of single flux quantum(SFQ) voltage pulse. By retiming, the number of flip flops is minimized through arrangement of the order of pulse arrivals of each gate. The result shows that most of the flipflops in the circuit are removed.

P.K. Meher and S. Y. Park, "Critical-Path Analysis and Low-Complexity Implementation of the LMS Adaptive Algorithm[4],” In this paper, authors shows that the direct-form(DF) and transpose-form(TF) Least mean square(LMS) adaptive filter have nearly the same critical path delay. They have presented three different structures of direct form Least Mean Square adaptive filter with zero adaptation delay, one adaptation delay, two adaptation delays are referred to as proposed Design 1, 2,3 where Design 1 having no adaption delay, design 2 having one adaption delay and Design 3 with two adaption delay. In proposed design one, does not involve any adaptation delay. The two main computing block in the direct form least mean square adaptive filter, namely the error-computation block and the weight-update block. We can be realized with a very small adaptation delay in cases where a very high sampling rate is required. In Proposed Design one, has the minimum MUF among all the structures and minimum area with minimum energy per sample(EPS). But Design 1 is adequate to support the highest data rate in current communication systems. When implement the least mean square algorithm, one has to update the filter which is equals to the difference between the desired response and the current filter output.

S. G. Ramasubramanian, S. Venkataramani, A. Parandhaman and A. Raghunathan, "Relax-and-Retime: A methodology for energy-efficient recovery based design[5]," S. G. Ramasubramanian, S. Venkataramani, A. Parandhaman and A. Raghunathan proposed the use of retiming, a well-known and powerful sequential optimization technique to redefine the boundaries of combinational logic, thereby creating new opportunities for Recovery Based Design that cannot be explored by previous techniques. They make the key observation that, in retiming circuits with Recovery Based Design , it is acceptable for a few paths in the circuit to exceed the clock period. Using this insight, this proposed a synthesis methodology, Relax-and-Retire, wherein the original circuit is relaxed by ignoring timing constraints on selected paths that are bottlenecks to retiming. When classical minimum period retiming is employed on this relaxed circuit, the path wall is shifted to a lower delay, thus allowing additional voltage overscaling. Their results demonstrate 9-25% (average of 15.3%) improvement in overall energy compared to a well-optimized baseline with Recovery Based Design.

V. Pandey, S. C. Yadav and P. Arora, “Retiming technique for clock period minimization using shortest path algorithm[6],” Computation time of digital circuit can be reduced by applying transformation of delay that is retiming to digital signal block, which can be applied to digital signal processing blocks that can reduce computation time. For transformation of delay they need critical path and shortest path computation algorithm. Clock period minimization techniques of retiming used to minimize clock period of the circuit like IIR, FIR filters. This paper computed critical path before applying retiming in circuit, it gives us an estimation of computing time. Shortest path algorithms are required in the circuit for solving shortest path problem in the graph. This explaining clock period minimization technique of retiming to enhance speed and proposing new shortest path algorithm and giving new Dijkstra algorithm because it has less run time complexity and high speed.Author also observed that most of filter data flow graph are sparse.

K. Qiu, M. Zhao, Q. Li, C. Fu and C. J. Xue, "Migration-Aware Loop Retiming for STT-RAM-Based Hybrid Cache in Embedded Systems[7]," In this research work presents the interesting observations the migration in stencil loops are significant. Architecture of Hybrid cache consist of spin-transfer torque RAM and SRAM and this paper proposed migration based techniques which is dynamically moves write-intensive and read-intensive data

between STT-RAM and SRAM. For stencil loops with read and write data dependencies, they observe that migration overhead is significant, and migrations closely correlate to the interleaved read and write memory access pattern in a memory block. This paper proposes a loop retiming framework during compilation to reduce the migration overhead by changing the interleaved memory access pattern. With the proposed loop retiming technique, the interleaved memory accesses can be significantly reduced so that migration overhead is mitigated, and energy efficiency of hybrid cache is significantly improved.

Amala Maria Alex, Nidhish Antony, "Design of Modified Low Power and High Speed Carry Select Adder Using Brent Kung Adder[8]" In order to perform the addition of two numbers adder is used. Adder also forms the integral part of ALU. Different algorithm in Digital Signal Processing such as FIR and IIR are also employed using adder. The important areas of VLSI areas are low power, high speed and data logic design. In Carry Select adder the possible value of input carry are 0 and 1. So in advance, the result can be calculated. Further they have the multiplexer stage, for calculating the result in its advanced stage. Here, one RCA is replaced by Brent kung adder. In proposed model a modification is done by using D-LATCH instead of Binary to Excess-1 to improve the speed and reduce power. Here the Binary to Excess-1 Converter is replaced with a D-Latch. Initially when en=1, the output of the BK adder is fed as input to the D-Latch and the output of the D-latch follows the input and given as an input to the multiplexer. When en=0, the last state of the D input is trapped and held in the latch and therefore the output from the BK adder is directly given as an input to the Mux without any delay.

M. Jayashree, " Design of High Speed and Area Efficient FIR Filter Architecture using modified Adder and Multiplier[9]" In this work, proposed design of digital Finite Impulse Response filter using VHDL. It is implemented by Xilinx 12.4 software. In this project introduce a Multiplier with SQRT CSLA to increase the performance of Multiplication and Accumulation(MAC) unit of Finite Impulse Response. In this paper, the existing adder is Ripple carry adder and is replaced square root carry select adder and the performance is compared and as the modified adder has improved performance and to reduce the drawbacks. The reduction of area delay and power is identified for reduce complexity SQRT CSLA based Bi-recoder multiplier and the finite impulse response filter output using two different multiplier is compared.

IV. PROPOSED METHODOLOGY

In this research examination work minimum clock period measured optimized retiming of FIR circuit using Brent Kung Adder for filter length 8 and 16 has proposed and implemented on Xilinx13.1 design suite.

Steps of implementation of a proposed design using Xilinx ISE in hardware description language. The steps involved in implementation of proposed design are briefed as follows:

Step 1: Create New Project: Using Xilinx ISE design suite create a new project in project navigator and select target device to implement project.

Step 2: Write program for proposed design in Verilog HDL (hardware description language) specify IO ports. Using mixed modeling style of hardware design describe behavioral and structural design of proposed model. To model a parallel prefix BK adder functions for all three stages are discussed in equation.

Step 3: Save and Check Syntax: Save written program for proposed design and check for syntax error.

Step 4: Synthesis: Run behavioral synthesis to implement behavior of proposed design in to hardware and generate Xst file and Netlist file.

Step 5: View RTL schematic and technology schematic of implemented design in Xilinx to examine and compare with model design to verify.

Step 6: Verification: To verify proposed design testbench are created in UVM . To verify using testbench, random simulates are provided and results are examined and compared with expected outcome or standard outcome. The testbench verification shows that proposed design shows expected behavioral functionally defined by user.

Step 7: View synthesis summary to examine device utilization and critical delay in circuit. Compare results with existing previous work with respect to LUTs, FF, and delay in ns.

V. CONCLUSION

In this work an FIR filter designed by using Brent kung adder to increase the speed and to reduce complexity. Brent kung adder is used because it processes in a parallel manner and the output can be easily obtained. By doing so we are increasing the speed of the process. This work presented a MCP optimized of Finite Impulse Response Filter using Brent Kung Adder considering seamless signal propagation in circuits, which provides a simple way to obtain adequately precise estimate of propagation delays across different paths in a DFG. Delay element is also compared between Ripple Carry Adder and Brent Kung Adder, which shows that Brent kung adder is low delay than Ripple Carry Adder.

This technique of fixed points circuits can be extended to floating point circuits. In FIR Filter, Adder and Multiplier can be change.

REFERENCES

[1] P. K. Meher, "On Efficient Retiming of Fixed-Point Circuits[1]," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 4, pp. 1257-1265, April 2016. doi: 10.1109/TVLSI.2015.2453324

[2] S. Guo et al., "A low-power 28 Gb/s CDR using artificial lc transmission line technique in 65 nm CMOS," 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station, TX, 2014, pp. 85-88.doi: 10.1109/MWSCAS.2014.6908358.

[3] N. Kito, K. Takagi and N. Takagi, "Conversion of a CMOS Logic Circuit Design to an RSFQ Design Considering Latching Function of RSFQ Logic Gates," in IEEE Transactions on Applied Superconductivity, vol. 25, no. 3, pp. 1-5, June 2015.doi: 10.1109/TASC.2014.2378593.

[4] P. K. Meher and S. Y. Park, "Critical-Path Analysis and Low-Complexity Implementation of the LMS Adaptive Algorithm," in IEEE Transactions on Circuits and Systems I: Regular Research works, vol. 61, no. 3, pp. 778-788, March 2014.doi: 10.1109/TCSI.2013.2284173

[5] S. G. Ramasubramanian, S. Venkataramani, A. Parandhaman and A. Raghunathan, "Relax-and-Retime: A methodology for energy-efficient recovery based design," 2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC), Austin, TX, 2013, pp. 1-6.doi: 10.1145/2463209.2488871

[6] V. Pandey, S. C. Yadav and P. Arora, "Retiming technique for clock period minimization using shortest path algorithm," 2016 International Conference on Computing, Communication and Automation (ICCCA), Noida, 2016, pp. 1418-1423.

[7] K. Qiu, M. Zhao, Q. Li, C. Fu and C. J. Xue, "Migration-Aware Loop Retiming for STT-RAM-Based Hybrid Cache in Embedded Systems," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 33, no. 3, pp. 329-342, March 2014.

[8] Amala Maria Alex, Nidhish Antony, “Design of Modified Low Power and High Speed Carry Select Adder Using Brent Kung Adder” vol.1,pp. 196-204

[9] M. Jayashree, “Design of High Speed and Area Efficient FIR Filter Architecture using modified Adder and Multiplier” International Journal of Engineering and Techniques-vol.4 issue 3, May 2018

[10] O. Sinanoglu and V. D. Agrawal, "Retiming scan circuit to eliminate timing penalty," 2012 13th Latin American Test Workshop (LATW), Quito, Ecuador, 2012, pp. 1-6.

[11] C. E. Leiserson and J. B. Saxe, “Retiming synchronous circuitry,” Algorithmica, vol. 6, nos. 1-6, pp. 5-35, Jun. 1991.

[12] K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation. New York, NY, USA: Wiley, 2007.

[13] P. K. Meher, “Seamless pipelining of DSP circuits,” J. Circuits Syst. Signal Process., Jul. 2015. [Online]. Available: http://link. springer.com/article/10.1007%2Fs00034-015-0089-2.

[14] R. Dhivya and Dr. P. Brindha, “ Design and Implementation of FIR Filter using Retiming Technique”, IJARIIT ISSN: 2454-132X, vol.3 2017.

[15] S.V Padmajarani and M Murlidhar, “ Comparison of Parallel Prefix Adders Performance in an FPGA”, International Jounal of Engineering Research and Development(IJERD), Vol 3, No.6, pp. 62-67, September-2012.

[16] R. Mahesh and A. P. Vinod, ―New reconfigurable architectures for implementing FIR filters with low complexity,‖ *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, vol. 29, no. 2, pp. 275–288, Feb. 2010.

[17] Sudheer Kumar Yezerla, B RajendraNaik, “Design and Estimation of Delay, Power and Area for Parallel prefix adders”, proceedings of 2014 RAECS UIET Panjab University Chandigarh, 06-08 March,2014.

[18] L. Ciminiera, P. Montusuchi, “Carry-Save Multiplication Schemes Without Final Edition”, IEEE Transaction on Computer, vol.45, no.9, Sep.1996.