# Review paper on DIT & DIF Radix-2 Fast Fourier Transforms and Its FPGA Implementation

Furkan Alam[1], Prof. Suresh. S. Gawande[2], Prof. Satyarth Tiwari[3]

*[1]M. Tech. Scholar, [2]Guide, [3]Co-guide*

*Department of Electronics and Communication, Bhabha Engineering Research Institute, Bhopal*

***Abstract*—The Fast Fourier transform (FFT) is an as often as possible utilized Digital signal processing (DSP) calculations for the uses of Orthogonal Frequency Division multiplexing (OFDM). The blend of Orthogonal Frequency Division Multiplexing (OFDM) with Multiple Input Multiple Output (MIMO) signal handling is a clear approach of upgrading the information rates of different correspondence frameworks, for example, Wireless LAN, e Mobile, 4G and so on. Since FFT processor is an intricate module in OFDM, it is exceedingly unavoidable to plan the processor in a productive way. This research work involved the implementation of a low delay and area efficient radix-2 decimation in time (DIT) using 8-point, 16-point, 32-point, 64-point and 128-point algorithm using radix-2 butterfly. In this paper is used unsigned, signed and complex number for radix-2 algorithm.***

***Index Terms*— FFT, Decimation in Time, Decimation in Frequency, real Value data**

## I. INTRODUCTION

Digital signal processing (DSP) is the scientific control of a data sign to adjust or enhance it somehow. It is portrayed by the representation of discrete time, discrete recurrence, or other discrete area signals by a succession of numbers or images and the preparing of these signs [1].

The objective of DSP is for the most part to quantify, channel and/or pack nonstop genuine simple signs. The initial step is for the most part to change over the sign from a simple to an advanced structure, by inspecting and after that digitizing it utilizing a simple to-computerized converter (ADC), which transforms the simple sign into a surge of numbers. Be that as it may, regularly, the required yield sign is another simple yield signal, which requires an advanced to-simple converter (DAC). Regardless of the fact that this procedure is more mind boggling than simple preparing and has a discrete worth range, the use of computational energy to advanced sign handling considers numerous points of interest over simple handling in numerous applications, for example, mistake recognition and revision in transmission and additionally information pressure. DSP calculations have for quite some time been keep running on standard PCs, and in addition on particular processors called advanced sign processor and deliberately assembled equipment, for example, applicationparticular coordinated circuit (ASICs). Today there are extra advances utilized for computerized signal preparing including all the more intense broadly useful chip, field-programmable gate array (FPGAs), advanced sign controllers (generally for mechanical applications, for example, engine control), and stream processors, among others [2-3]. The FFT is a standout amongst the most normally utilized advanced sign preparing calculation. As of late, FFT processor has been generally utilized as a part of advanced sign handling field connected for OFDM, MIMO-OFDM correspondence frameworks.

FFT/IFFT processors are key segments for an orthogonal recurrence division multiplexing (OFDM) based remote IEEE 802.16 broadband correspondence framework; it is a standout amongst the most unpredictable and concentrated calculation module of different remote guidelines physical layer (ofdm802.11a, MIMO-OFDM 802.11, 802.16,802.16e) [4]. Some collapsed pipeline models have been proposed for the calculation of RFFT [3], [4], where butterfly operations are multiplexed into a little rationalunit. The structures in [3] and [4] could give satisfactory throughput to a few applications yet the capacity multifaceted nature of those structures keeps on being high. A couple set up structures has additionally been proposed for RFFT utilizing particular pressing calculations [5], [6]. Memory-struggle for read/compose operation is observed to be the significant test in the outline of calculations and structures for set up calculation [7]. As of late, a set up engineering and strife free memory tending to conspire have been proposed for persistent preparing of RFFT [8].

The FFT calculations are arranged into two general classes, to be specific, the decimation in-time (DIT) and the decimation in-frequency (DIF) calculations. The key contrastbetween the two are appeared in Fig. 1. If there should arise an occurrence of DIF calculation (Fig. 1(a)), the info tests are bolstered to the registering structure in their regular request, while the yield is created in bit-switched request. Then again, if there should be an occurrence of DIT calculation (Fig. 1(b)), the info tests need bit-inversion reordering before being handled, while the yield FFT coefficients are created in characteristic request. In various RFFT applications, for example,

picture and video handling, biomedical sign preparing, and time-arrangement investigation and so forth., the complete info grouping is for the most part accessible together in the meantime for the FFT calculation. The DIT RFFT has an advantage over the DIF form for these applications, since a DIT RFFT structure need not wait for the arrival of input samples but can produce the outputs as soon as those are computed.


(a) (b)

Figure 1: (a) DIF FFT butterfly (b) DIT FFT butterfly

## II. LITERATURE REVIEW

Pramod Kumar Meher et al. [7], the pulverization in-time (DIT) Fast Fourier Transform (FFT) frequently has advantage over the annihilation in-repeat (DIF) FFT for most certifiable regarded applications, like talk/picture/video dealing with, biomedical sign getting ready, and time-game plan examination, etc., since it doesn't require any yield reordering. Besides, the DIT FFT butterfly incorporates less estimation time than its DIF accomplice. In this paper, we show a viable building for the radix-2 DIT certifiable regarded FFT (RFFT). We display here the fundamental numerical enumerating for ousting the redundancies in the radix-2 DIT RFFT, and present a definition to regularize its stream diagram to empower fallen estimation with a direct control unit. We propose here an enlist based limit diagram which incorporates basically less zone to the detriment of fairly higher dormancy differentiated and the conventional RAM-based limit. The area time for crumbled set up DIT RFFT estimation with enroll based limit is taking a stab at following both read and create activities are performed in a similar time cycle at different zones. Thusly, we appear here a direct meaning of area time for the proposed radix-2 DIT RFFT structure. The proposed structure incorporates a 61% less area and 40% less power use than those of [8], everything considered, for FFT sizes 16, 32, 64, and 128. It incorporates 70% less zone postpone thing and 57% less imperativeness for each example than those of the other, everything considered, for the equivalent FFT sizes.

Manohar Ayinala et al. [8], this brief presents a novel adaptable building for set up snappy Fourier change (IFFT) figuring for real regarded signs. The proposed figuring relies upon a changed radix-2 computation, which removes the overabundance tasks from the stream graph. Another dealing with segment (PE) is proposed using two radix-2 butterflies that can system four contributions to parallel. An epic conflict free memory-tending to design is proposed to ensure the incessant task of the FFT processor. Furthermore, the tending to design is extended to reinforce various parallel PEs. The proposed real FFT processor in the meantime requires less estimation cycles and lower hardware cost appeared differently in relation to prior work. For example, the proposed framework with two PEs diminishes the figuring cycles by a segment of 2 for a 256-point certifiable speedy Fourier change (RFFT) appeared differently in relation to a prior work while keeping up lower gear unusualness. The amount of estimation cycles is diminished proportionately with the extension in the amount of PEs.

Shashank Mittal et al. [9], quick Fourier Transform (FFT) is a standout amongst the most fundamental and vital operation performed in Software Defined Radio (SDR). Consequently outlining a widespread, reconfigurable FFT calculation obstruct with low range, postpone and control necessity is critical. As of late it is demonstrated that Bruun's FFT is in a perfect world suited for SDR notwithstanding when working with higher piece exactness to keep up same NSR. In this paper, creators have proposed another engineering for Bruun's FFT utilizing an appropriated approach for increasing the quantity of bits (exactness) with progressive phases of FFT. It is likewise demonstrated that proposed engineering further lessens the equipment prerequisite of Bruun's FFT with immaterial changes in its NSR. The proposed outline makes Bruun's FFT, a superior choice for most useful cases in SDR. A point by point correlation of Bruun's customary and proposed equipment structures for same NSR is completed and consequences of FPGA and ASIC usage are given and talked about.

Byung G. Jo et al. [10], the paper proposes another persistent stream blended radix (CFMR) quick Fourier change (FFT) processor that utilizes the MR (radix-4/2) calculation and a novel set up technique. The current set up procedure bolsters just a settled radix FFT calculation. Interestingly, the proposed set up can bolster the MR calculation, which permits CF FFT calculations paying little heed to the length of FFT. The epic inplace technique is made by exchanging stockpiling areas of butterfly yields. The CFMR FFT processor gives the MR calculation, the set up system, and the CF FFT calculations in the meantime. The CFMR FFT processor requires just two - word recollections due to the proposed set up procedure. What's more, it utilizes one butterfly unit that can perform possibly one radix-4 butterfly or two radix-2 butterflies. The CFMR FFT processor utilizing the 0.18 m SEC cell library comprises of 37,000 doors barring recollections, requires just 640 clock cycles for a 512-point FFT and keeps running at 100 MHz. Consequently, the CFMR FFT processor can diminish equipment multifaceted nature and calculation cycles contrasted and existing FFT processors.

## III. FFT ALGORITHM

A quick Fourier change (FFT) is a calculation to process the discrete Fourier change (DFT) and its reverse. Fourier investigation changes over time (or space) to recurrence and the other way around; a FFT quickly registers such changes by factorizing the DFT framework into a result of scanty (for the most part zero) factors. Subsequently, quick Fourier changes are broadly utilized for some applications in building, science, and arithmetic. Demonstrate the butterfly tasks for radix-2 DIF FFT in figure 2 and figure 3. The radix-2 calculations are the most straightforward FFT butterfly calculation.

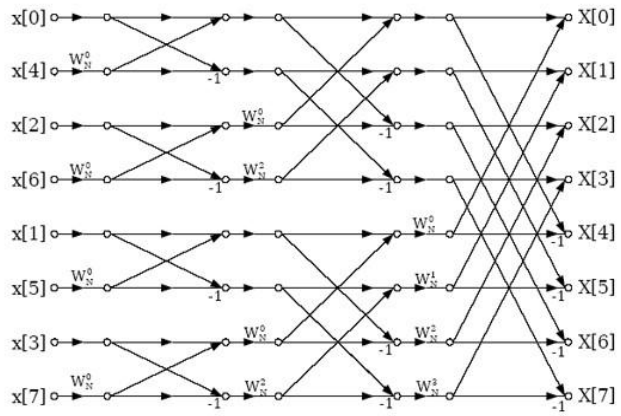


Figure 2: Radix-2 Decimation in Time Domain FFT

Algorithm

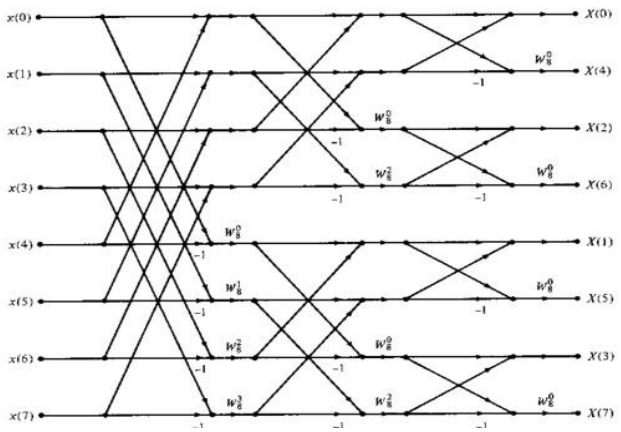


Figure 3: Radix-2 Decimation in Frequency Domain

FFT Algorithm

## IV. METHODOLOGY

**Array Multiplier:-**

Array multiplier is outstanding because of its standard structure. Multiplier circuit depends on include and move calculation. Every fractional item is created by the increase of the multiplicand with one multiplier bit. The fractional item are moved all to their bit request and afterward included.

**Complex multiplier:-**

Since complex increase is a costly activity, we will in general diminish the multiplicative multifaceted nature of the twiddle factor inside the butterfly processor by figuring just three genuine augmentations and three include/subtract tasks as in the twiddle factor duplication:

$$R + jI = (X + jY ).(C + jS) \quad (1)$$

However the complex multiplication can be simplified:

$$R = (C - S) .Y + Z \quad (2)$$

$$I = (C + S) .X - Z \quad (3)$$

With:

$$Z = C. (X - Y) \quad (4)$$

C and S are pre-computed and stored in a memory table. Therefore it is necessary to store the following three coefficients C, C + S, and C - S. The implemented algorithm of complex multiplication used in this work uses three multiplications, one addition and two subtractions as shown in Fig. 4.

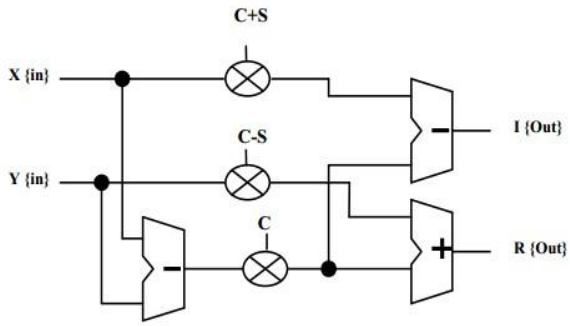


Figure 4: Implementation of complex multiplication

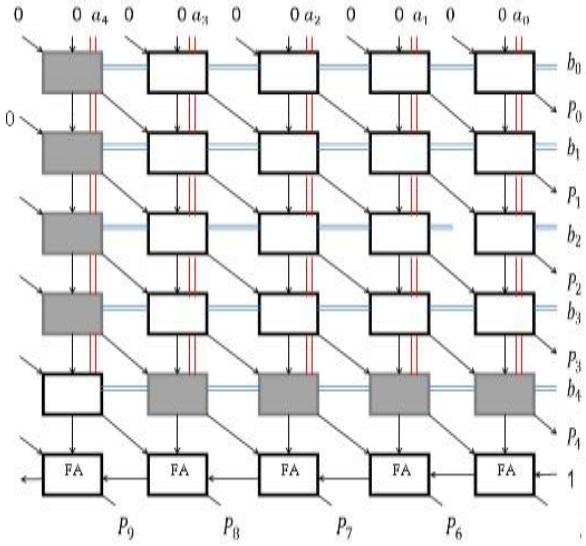


Figure 5: Baugh-Wooley Multiplier

**Baugh-Wooley :-**

Baugh-Wooley calculation for the marked double increase depends on the idea appeared in figure 5. The calculation

indicates that all conceivable AND terms are made first, and afterward sent through a variety of half-adders and full-adders with the Carry-outs anchored to the following most critical piece at each dimension of expansion. Negative operands might be duplicated utilizing a Baugh-Wooley multiplier.

**Adder/ Subtractor:-**

Input sequence of Conventional strategy is substantially more than to proposed technique, anyway proposed technique has less proliferation delay. Region and proliferation postponement can be diminished by the guide of changed kogge stone (KS) viper. This viper will be planned like as swell convey snake. Convey yield of one KS viper is associated with another KS snake yet this technique is extremely recipient for high productive advanced gadgets according to concerning engendering delay.

Inevitably, all the planning dimensions of advanced framework or IC's Packages rely upon number of entryways in a solitary chip that is additionally rung base methodology. Changed KS viper can be decreased with respect to the territory or number of doors. In the event that we expel the first XOR door from adjusted KS viper nothing will be changed for result however territory and proliferation defer will be decreased.

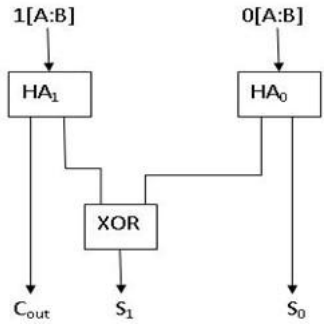


Figure 6:A Proposed 2 bit KS Adder

## V. EXPECTED OUTCOME

The proposed usage is customized (Described) and actualized utilizing VHDL dialect which is a Hardware Description Language that was produced by the Institute of Electrical and Electronic Engineers (IEEE) as a standard dialect for portraying the structure and conduct of advanced electronic frameworks. It has numerous highlights proper for depicting the conduct of electronic parts going from basic rationale doors to finish microchips and custom chips. The subsequent VHDL recreation models would then be able to be utilized as building hinders in bigger circuits (utilizing schematics, square outlines, or framework level VHDL portrayals) with the end goal of reenactment.

- Design 4-bit, 8-bit, 16-bit and 32-bit FFT with the help of logic gate and flip flop.
- All design are implemented using Xilinx Software for different device family (Spartan-6, Vertex-6 and Vertex-7) and calculate various parameter i.e.
- Number of Slice
- Number of LUTs
- Number of Flip Flop Pair
- Number of Input Output

All design will be compared with the previous base paper (2017) in different device family and achieved good result.

## VI. CONCLUSION

The prime objective is to construct a FFT in order to have low power consumption and lesser area. The parameters (i) power consumption (ii) Area occupancy were given due consideration for comparing the proposed circuit with other FFTs. The circuits were simulated using Model-Sim 6.3c and synthesized with Xilinx ISE 14.1.The performance of various 64 point FFT such as Radix-2, Radix-4, split Radix, mixed -radix 4-2, R2MDC and the proposed modified R2MDC were carried out and their performance were analyzed with respect to the number of CLB slices, utilization factor and Power consumption.

## REFERENCES

[1] Shaohan Liu and Dake Liu, “A High-Flexible Low-Latency Memory-Based FFT Processor for 4G, WLAN, and Future 5G”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume: 27 , Issue: 3 , PP. No. 513-523, March 2019.

[2] Basant K. Mohanty and Pramod Kumar Meher, “Area–Delay–Energy Efficient VLSI Architecture for Scalable In-Place Computation of FFT on Real Data”, IEEE Transactions on Circuits and Systems–I: Regular Papers, Vol. 42, Issue 9, September 2018.

[3] Charles. Roth Jr., “Digital Systems Design using VHDL”, Thomson Brooks/Cole, 7th reprint, 2005.

[4] S. S. Kerur, Prakash Narchi, Jayashree C N, Harish M Kittur and Girish V A, “Implementation of Vedic multiplier for Digital Signal Processing”, International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011, Proceedings published by International Joural of Computer Applications® (IJCA), pp.1-6.

[5] HimanshuThapaliyal and M.B Srinivas, “VLSI Implementation of RSA Encryption System Using Ancient Indian Vedic Mathematics”, Center for VLSI and Embedded System Technologies, International Institute of Information Technology Hyderabad, India.

[6] Jagadguru Swami Sri Bharati Krishna TirthajiMaharaja, "Vedic Mathematics: Sixteen simple Mathematical Formulae from the Veda", Delhi (2011).

[7] Harpreet Singh Dhillon and Abhijit Mitra, "A Reduced-bit Multiplication Algorithm for Digital Arithmetic", International Journal of Computational and Mathematical Sciences, Febrauary 2008, pp.6469.

[8] Sumit Vaidya and DepakDandekar. "Delay-power performance comparison of multipliers in VLSI circuit design". International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010.

[9] Pramod Kumar Mehe, Basant Kumar Mohanty,Sujit Kumar Patel, SoumyaGanguly, and ThambipillaiSrikanthan, *"*Efficient VLSI Architecture for Decimation-in-Time Fast Fourier Transform of Real-Valued Data*",* IEEE Transactions on Circuits And Systems—I: Regular Papers, Vol. 62, No. 12, December 2015.

[10] B. G. Jo and M. H. Sunwoo, "New continuous-flow mixed-radix (CFMR) FFT processor using novel in- place strategy," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 5, pp. 911–919, May 2005.