An Event Based CMOS Quad Bilateral Combination With Asynchronous SRAM Architecture Based Neural Network

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Abstract - NEURAL networks have a wide range of applications in analog and digital signal processing. Once the network has been trained and the synaptic weight values stored in the SRAM, the VLSI device can be used in stand-alone mode to carry out neural computation in real-time. In existing system they implemented the neural network with programmable synaptic memory. Synaptic weight refers to the strength of a connection between two nodes. The design of neural network architecture is based on CMOS technology and the design performed in its architecture level. Commonly CMOS technology provides less noise during design. The proposed neural network consists of Synaptic weight and spiking network. In the existing system, they concentrated only in spike frequency and spike voltage. The proposed system focuses on reducing the complexity and increasing the efficiency and the network using CMOS technology with quad bilateral technique used in integrated circuit designed to reduce power consumption, by shutting off the current to block the circuits that are not in use and also multiple threshold voltages applied to the circuit which helps to reduce the delay/power. In addition to reducing stand-by or leakage power this approach eliminates critical path delay. The proposed design concentrates on reducing complexity; hence the power consumption will be reduced and also efficiency will be increased due to less complexity. The proposed system can be used in image processing & control system applications.

Keywords: Neural networks, analog, digital, synaptic weight, Static Random Access Memory (SRAM), Very Large Scale Integrated Circuit (VLSI), neural network, programmable synaptic memory, spiking network, spike frequency, spike voltage, quad bilateral technique and multiple threshold voltage.

I. INTRODUCTION

NEURAL networks have a wide range of applications in analog and digital signal processing. A lot of research has been done in digital implementation of multipliers and adders, memory architecture which can be readily used leaving the nonlinear activation function as the most complex building blocks in spiking neural network. [1]

Spiking neural networks represent a promising computational paradigm for solving complex pattern recognition and sensory processing tasks that are difficult to tackle using standard machine vision and machine learning techniques. [1]

A general framework which encompasses the training of neural networks and the adaptation of filters. Data show that biological synapses behave quite differently from the symbolic synapses in all common artificial neural network models. In particular, we analyze computations on temporal and spatiotemporal patterns, and we give a complete mathematical characterization of all filters that can be approximated by feed forward neural networks with dynamic synapses. [2]

A silicon neuron circuit that produces spiking and bursting firing patterns, with biologically plausible spike shape, is presented. The circuit mimics the behavior of known classes of cortical neurons: regular spiking (RS), fast spiking (FS), chattering (CH) and intrinsic bursting (IB). [8]

The network is made of integrate-and-fire neurons with constant leak and a floor. The synapses are bistable, and they are modified by the arrival of pre synaptic spikes. The sign of the change is determined by both the depolarization and the state of a variable that integrates the post synaptic action potentials. The absence of stimulation, the synapses preserve their internal state indefinitely. Memories are also very robust to the disruptive action of spontaneous activity. [5]

II. SYSTEM MODEL

Asynchronous programmable synaptic memory is used for compact full-custom VLSI device that comprises low-power sub-threshold analog circuits. It is used spike timing dependent plasticity algorithm. In this algorithm

dependence on both the postsynaptic depolarization and the frequency of pre and postsynaptic neurons.

The asynchronous communication scheme implemented in this VLSI device is based on the Address Event Representation (AER) communication protocol, commonly used to build large scale multi chip neuromorphic systems.

The membrane potential is then reset to the neuron's tunable reset potential. The neuron circuit is the "Adaptive exponential I&F neuron" described in but with an extra free parameter corresponding to the neuron's reset potential.

In the asynchronous programmable synaptic memory is an exponential rise due to the negative feedback in the silicon neuron's circuit that causes the neuron to generate an action potential.

Asynchronous SRAM architecture is used for quad bilateral technique. In this technique is a qualified for automotive applications. Fast switching, propagation speeds and low OFF leakage current. CMOS Quad bilateral combination contains four independent digitally controlled analog switches that use silicon-gate CMOS technology.

CMOS quad bilateral technique is used to reduce the no of transistors in the neuron circuit. It is used to optimize the switching activity SRAM CMOS architecture and modify the CMOS cell interconnection for the switching network.

In the asynchronous SRAM architecture is an exponential rise due to the positive feedback in the silicon neuron's circuit that causes the neuron to generate an action potential.

III. PREVIOUS WORK

The existing system device comprising both, a neuromorphic "neuron core", with biophysically realistic analog synapse and neuron circuits, as well as a fully asynchronous digital memory block. The neural-core block comprises 32 Integrate-and-Fire (I&F) neurons, four synapse circuits (three excitatory and one inhibitory) per neuron, and a synapse address demultiplexer circuit.

From figure: 1 shows chip block diagram. The device comprises a neural-core module with an array of synapses and integrate-and-fire neurons, an asynchronous SRAM module to store the synaptic weight values, a bias generator to set the parameters in the analog circuits, and asynchronous control and interfacing circuits to manages the AER communication.

The demonstrate that input events are successfully transmitted through the input Address Event representation (AER) stages onto the SRAM block, that the SRAM provides in output the expected bits, that the synapse converts the stored digital word into a properly weighted synaptic current.

The synaptic currents get properly integrated by the spiking neurons and that the spikes get properly converted into AER events and transmitted by the output AER stages.

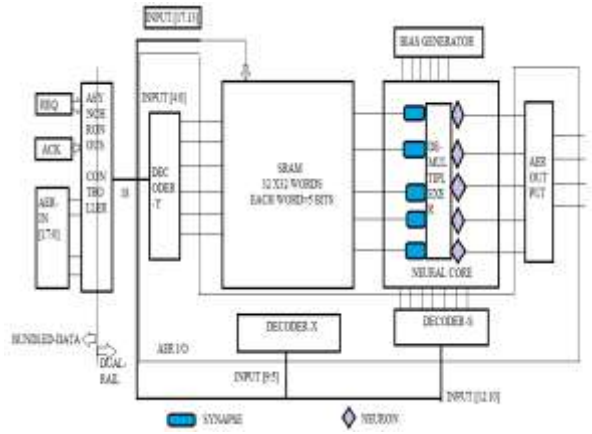

Figure 1: block diagram of existing system

IV. PROPOSED METHODOLOGY

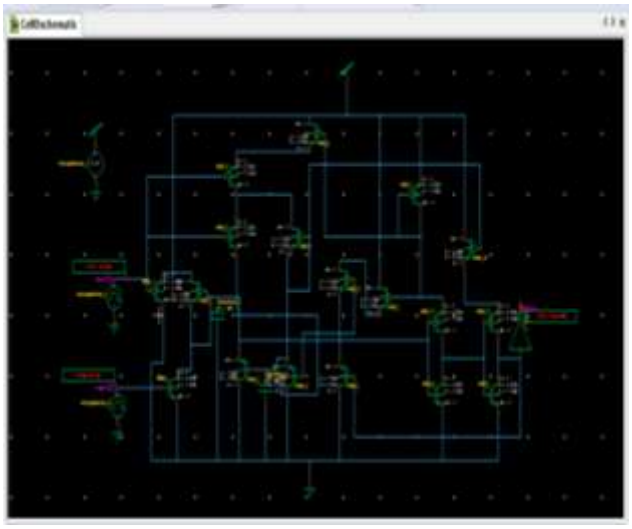

Figure 2: circuit design

From figure: 2 the circuit design of neural network.

An input DPI low-pass filter implements the neuron leak conductance. A non-inverting amplifier with current-mode positive feedback produces address-events at extremely low-power operation.

A reset block resets the neuron to the reset voltage and keeps it reset for a refractory period, set by the bias voltage. An additional DPI low-pass filter integrates the output events in a negative feedback loop, to implement a spike-frequency adaptation mechanism.

The neuron circuit can implements the CMOS quad bilateral technique. The neuron circuit focuses on reducing the complexity and increasing the efficiency and the network using CMOS technology with quad bilateral technique used in integrated circuit designed to reduce power consumption, by shutting off the current to block the circuits that are not in use and also multiple threshold voltages applied to the circuit which helps to reduce the delay/power.

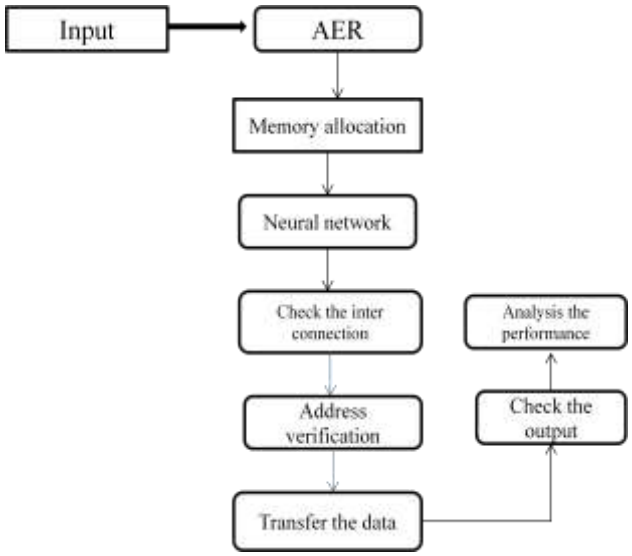

Figure 3: flow diagram of proposed system

From figure: 3 the flow diagram generate the process of neural network.

SRAM is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. Two important characteristics of CMOS devices are high noise immunity and low static power consumption.

CMOS allows a high density of logic functions on a chip.SRAM exhibits data remanence but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

The SRAM architecture is two row and column decoders receive five bits each, encoded in dual-rail, and generate a one-hot code at the output. The content of the memory block is programmed by setting the Write enable signal to VDD and transmitting the five bits that represent the content of the memory cells together with the standard address-event data.

The neuron circuit is the "Adaptive exponential I&F neuron" described in but with an extra free parameter corresponding to the neuron's reset potential. When a neuron fires, it generates a signal which travels to other neurons, which, in turn, increase or decrease their potentials in accordance with this signal.

This circuit is a digital programmable switch-matrix that re-configures the connectivity between the synapse output nodes with neuron input ones. In its default configuration the synapse output nodes of each row are connected to the neuron input node of the same row, therefore giving rise to a network of 32 neurons, each receiving 4:32 virtual synaptic inputs (4 synapse types and 32 synaptic weights, stored in the SRAM cells).

V. SIMULATION RESULTS

The proposed system produces better results when compared to the existing method. The gate count value reduces from 21 to 18.The power value has been reduced from 12mW to 150uW. The area value has been reduced from 28mX21m to 28mX20m.

TABLE: 1 COMPARISON TABLE

TABULATION FOR POWER AND GATE COUNT FOR EXISTING AND PROPOSED SYSTEM

Method	**Existing**	**Proposed**
Area	28m X 21m	28m X 20m
Power	12mW	150uW
Gate count	21	18

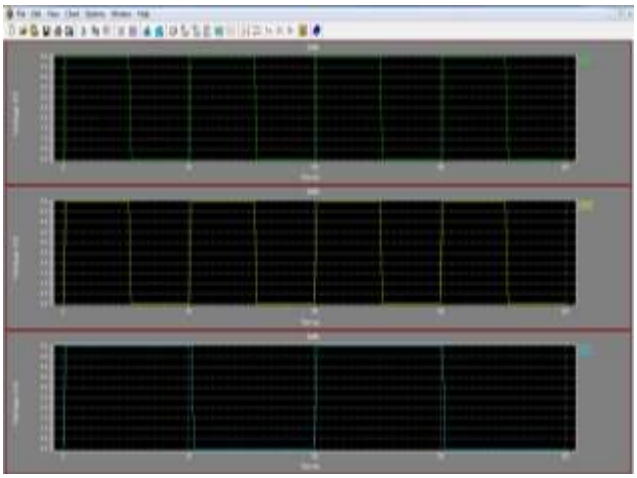

Figure 4: Output waveform of proposed system

From figure: 4 the output waveform obtained due to implementation of quad bilateral technique.

VI. CONCLUSION

A novel neuromorphic VLSI device comprising both a spiking neural-core with biophysically realistic analog synapse and neuron circuits, as well as a fully asynchronous digital memory block. The interface to the SRAM block and the SRAM itself could be done off-chip Programmable Gate Array verified in this prototype chip the correct functionality of the new asynchronous SRAM interfacing circuits. The values for parameters such as power, delay and gate count gets reduced by implementing quad bilateral technique.

VI. FUTURE SCOPES

In future, the design can be extended by using the low flicker noise ASIC preamplifier. This may optimize the networks and reduce the power consumption compare to the previous system which results in optimized neural network for SRAM architecture. It can also be extended to areas like Broad spectrum of data intensive application, Control systems and Image processing application

VII. REFERENCES

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