Equivalence of Domino Circuits for 8-bit and 16-bit OR Gates

T. Latha[#], T. Suresh Babu*
[#]*ECE Dept (M.E-VLSI Design),* [#]*Assistant Professor (ECE Dept)*

Abstract - In this paper, several domino circuits are compared with proposed technique such as current comparison based domino circuit. The proposed domino circuit has lower leakage power and higher speed for wide fan-in gates and which is based on the keeper circuit and comparison of mirrored current of the pull-up network with its worst case leakage current. The current comparison based domino circuit decreases the parasitic capacitance on the dynamic node, generating a smaller keeper for wide fan-in gates to implement fast and robust circuits. Thus the power consumption and delay are reduced. The leakage power is also reduced. Simulation results of wide fan-in gates are designed using an 180nm technology. The static power, dynamic power, leakage power and delay are compared with the various domino circuits for 8-bit and 16-bit OR gates.

Keywords: Domino logic, Leakage-tolerant, Keeper, Wide fan-in, Current mirror.

I. INTRODUCTION

Power consumption is one of the top concerns of VLSI circuit design, for which CMOS is the primary technology. Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching and static power is consumed regardless of transistor switching. Leakage and noise margin problems are addressed by keeper circuit. If a dynamic node is precharged high and left floating, then the voltage on the dynamic node will drift over time due to gate, sub threshold junction leakages [1]. The keeper must be wide to compensate for any leakage current when the output is floating and pull down network is off. Noise margin can be improved by using strong keepers. Fan-in is the numbers of inputs a gate can handle. Physical logic gates with a large fan-in tend to be slower than those with a small fan-in.

This is because the complexity of the input circuitry increases the input capacitance of the device. Using logic gates with higher fan-in will help reducing the depth of a logic circuit. More static power is consumed by pseudo–NMOS gates. So, if they are not needed, they turned off to reduce the static power. Sub threshold leakage power is a very big problem in the battery design. It can be controlled through the body voltage using the body effect. Dynamic power is depend on the activity factor, clock frequency and switching capacitance. If the chip is active dynamic power dissipation is high. The power is reduced by reducing frequency and voltage. The current being copied can be, and sometimes is, a varying signal current. The current mirror is used to provide bias currents to circuits. In this paper, various domino circuit performances were compared. Their respective delays and power consumption have been calculated and compared in cadence virtuoso tool at 180 nm CMOS technology.

The rest of this paper is organized as follows. The system model is explained in section II. The previous work circuit designing and its operations are described in section III. Section IV explains the proposed technique. Section V includes simulation results and the proposed circuit is compared with other domino circuits for 8-bit and 16-bit . After the conclusion in section VI, the future scope is included in section VII.

II. SYSTEM MODEL

The main source of noise in deep-submicron circuit is mainly due to the higher leakage current, crosstalk, supply noise and charge sharing, while noise at the input of the evaluation transistor may increases due to increased crosstalk. The leakage immunity is more problematic in high fan-in domino circuits because of larger leakage due to more parallel evaluation paths. The several Domino circuits have number of NMOS inputs. These circuit techniques are divided into two categories. The first category, circuit techniques such as Conditional keeper domino [2], High speed domino [3], LCR keeper domino [4], Controlled keeper by current comparison domino [5], Standard footer less domino & Diode footed domino [6], Diode partitioned domino [7] are used. In the second category, circuit technique Current comparison based domino [8] is used.

III. PREVIOUS WORK

A. Conditional Keeper Domino

The conditional keeper circuit Fig. 3.1 Works as follows: at the beginning of the evaluation phase, the smaller keeper (K1) is ON for keeping the state of the dynamic node. After the delay inverters if the dynamic node is still high, the output of the NAND gate goes low and K2 is ON.

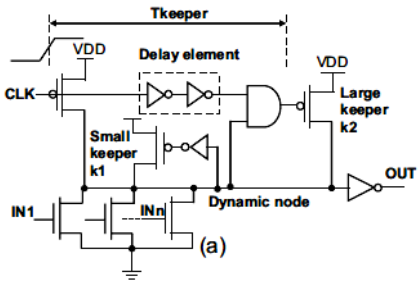

Fig. 3.1 CKD circuit

This keeper transistor is in larger size when compared to K1 transistor. The keeper maintains the state of the dynamic node for the rest of the evaluation period as explained in [2].

B. High Speed Domino

The high speed domino circuit at the beginning of the evaluation phase, the input delay element is low and the clock is high in Fig. 3.2 PMOS transistor MP3 is ON and therefore it turns OFF the keeper transistor MP2. After a delay equal to the delay of the inverters, when clock delayed is high, if the output node is high, MN1 remains in the OFF state and keeper transistor MP2 also remains OFF. This causes PMOS transistor MP2 (keeper transistor) to be turned ON to keep the dynamic node strongly connected to VDD.

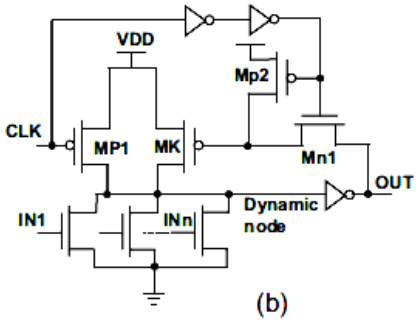

Fig. 3.2 HSD circuit

The turned OFF keeper transistor at the beginning of the evaluation phase helps to remove the contention between the keeper and NMOS evaluation network, thus achieving less power consumption and higher performance[3]. However, the dynamic node is floating at the beginning of the evaluation phase since the keeper is turned OFF. Therefore, if there is noise at the inputs at the onset of evaluation, the dynamic node can be discharged.

C .Leakage current Replica Keeper Domino

The leakage current replica (LCR) keeper for dynamic domino gates that uses an analog current mirror to replicate the leakage current of a dynamic gate pull-down stack and thus tracks process, voltage, and temperature Fig. 3.3 The LCR keeper uses a conventional analog current mirror that tracks any process corner as well as voltage and temperature. The only variation that the LCR keeper cannot track is random on-die variation, which still must be addressed using conventional margining. The leakage current replica keeper is used to improve the scaling of the dynamic gates. A single current mirror structure can be shared among more than one dynamic gate, as explained in [4]. The LCR keeper overhead is one pFET per dynamic gate plus a portion of the shared current mirror circuit. The LCR keeper requires an overhead of one FET per dynamic gate plus a portion of a shared replica current mirror.

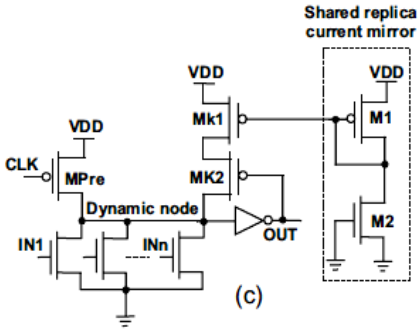

Fig. 3.3 LCR keeper domino

D .Controlled Keeper by Current Comparison Domino

The voltage of the dynamic node is mainly decreased to zero in two different states: either a conduction path to the ground is formed by the input vector or the leakage current of the pull down network with OFF transistors is increased that discharges the dynamic node due to the increased temperature or the existence of several parallel (leakage) paths from the dynamic node to the ground in Fig. 3.4 The

keeper transistor should not turn off in the latter state. However, the current in the former state is more than the other. Therefore, the only way to distinguish between the two states is use of a reference current, which corresponds to the pull down network leakage and the temperature of the chip [5].

The reference current is compared with the pull down network current. If there is no conducting path from the dynamic node to the ground and the only current in the pull down network is the leakage current, the keeper transistor will not turn off because the reference current is greater than the leakage current.

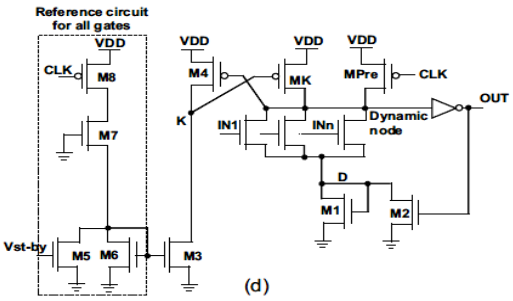

Fig 3.4 CKCCD circuit

E. Standard Footer less Domino

A domino logic circuit includes a pre-charge circuit pre-charging a dynamic node in response to a clock signal. This circuit is most popular dynamic logic is the conventional standard domino circuit as shown in Fig. 3.5The footer less domino circuit is providing the high speed performance over the footed domino logic [6]. However, adding the PMOS keeper transistor degrades the performance and increases the power dissipation in the circuit. Upsizing the keeper transistor is one of the ways to improve the robustness and it increase the current contention between the keeper transistor and the evaluation network.

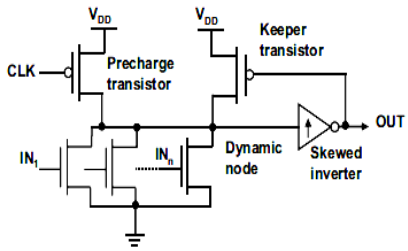

Fig. 3.5 SFLD circuit

F. Diode Footed Domino

We modify the domino circuit by adding an NMOS transistor in a diode configuration (gate and drain terminals connected together) in series with the evaluation network, as illustrated in Fig. 3.6. The diode footer (transistor M1) decreases the subthreshold leakage due to a phenomenon called the stacking effect. Due to the leakage of the evaluation transistors, there is some voltage drop established across the diode footer (transistor M1) in the evaluation phase. The diode footer increases the switching threshold voltage of the gate by the threshold of NMOS devices [6].

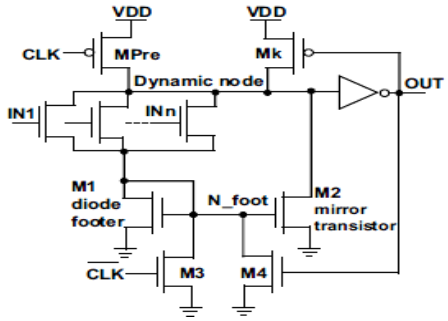

Fig. 3.6 DFD circuit

The higher gate switching voltage results in a better noise immunity, however, at the expense of performance degradation. The reason for performance degradation is that the diode footer decreases the evaluation current. This circuit is more immune to noise compared to footer less domino logic. The noise immunity is higher because of using footer transistor at the bottom of the evaluation network. The speed is lower than footer less domino logic.

G. Diode Partitioned Domino

Diode partitioned domino, the enhanced diode divides and reduces the parasitic capacitance on the domino node as shown in Fig. 3.7 The diodes separates node into two partitions. With the worst case input, only path turns on and partition becomes active.

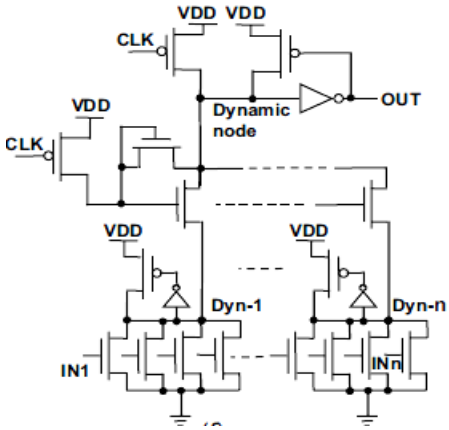

Fig. 3.7 DPD circuit

The other NMOS paths are turned off. Path discharges but does not affect due to the reverse connection of the diode. The parasitic capacitance of is divided into diodes, as explained in [7]. The DP domino does not only divide the parasitic capacitance but also divides the keeper transistors.

IV. PROPOSED METHODOLOGY

The wide fan-in dynamic gates, especially for wide fan-in OR gates, robustness and performance significantly degrade with increasing leakage current. A new current-comparison-based domino (CCD) circuit for wide fan-in applications in ultra deep sub micrometer technologies which is used to increases performance and decreases leakage power consumption [8].

In Fig. 4.1, Transistor M_K is added in series with the reference current to reduce power consumption when the voltage of the output node has fallen to ground voltage. This circuit is similar to a replica leakage circuit, in which a series diode-connection transistor M_6 similar to M_1 is added. This circuit was a replica of the worst case leakage current of the Pull up network to correctly track leakage current variations due to process variations [4]. Therefore, the gate of transistor M_7 is connected to V_{DD}, and its size is derived from the sizes of PMOS transistors of the Pull up network in the worst case, i.e., a n-input OR gate, and hence its width is set equal to the sum of the widths of n PMOS transistors of the pull up network.

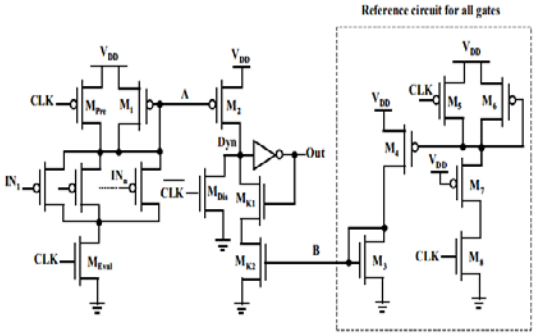

Fig. 4.1 Wide OR gate using CCD

The CCD circuit can be considered as two stages. The first stage pre-evaluation network includes the Pull up network and transistors M_{Pre}, M_{Eval}, and M_1. The second stage looks like a footless domino with one input, without any charge sharing, one transistor M_2 regardless of the implemented Boolean function in the Pull up network, and a controlled keeper consists of two transistors. Transistor M_1 is configured in diode connection, i.e., its gate and drain terminal are connected together. The reference current circuit act as the shared replica current mirror and it is used to copy the current from one active device to by controlling the current in another active device of a circuit.

In the evaluation mode, the current of the Pull up network transistors establishes some voltage drop across M_1. This voltage will be low, if all inputs are at the high level and only leakage current exists in the pull up network and mirror transistor M_2. This circuit has been more robustness with low leakage. The footer transistor are used to reduce the leakage current and increased in noise immunity [4].

Pre-charge Phase

In this phase, clock voltage is in the low level and input signals can be in the high level. Hence, transistors M_{pre}, M_D is, M_{k1}, and M_{k2} are on and transistors M_1, M_2, and M_{Eval} are off.

Evaluation Phase

In this phase, clock voltage is in the high level and input signals can be in the low level. Hence, transistors M_{pre} and M_D is are off, transistor M_2, M_{k2}, and M_{Eval} are on, and transistor M_{k1} can become on or off depending on input voltages.

V. SIMULATION /EXPERIMENTAL RESULTS

A. Output for Various Domino Circuits

When the clock is low it goes to pre-charge phase. The clock is low-to-high it goes to evaluation phase Fig. 5.1 Various domino circuits outputs are depend on n-number of inputs in the evaluation network. This methodology is based on the wide fan-in OR gate, so any one of the input is high the output goes to high.

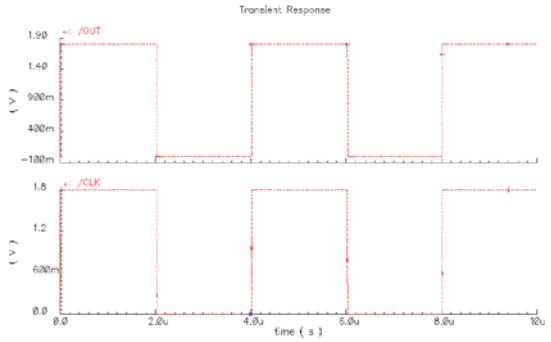

Fig.5.1 Output for domino circuits

B.Leakage Power Calculation

The power consumed by a device not related to state changes. Leakage power is actually consumed when a device is both static and switching, but generally the main concern with leakage power is when the device is in its inactive state, as all the power consumed in this state is considered "wasted" power. The Table 1 shows that the leakage power dissipation occurs in the different domino circuits for 8-bit and 16-bit.

TABLE 1. LEAKAGE POWER CALCULATION

S.No	Domino circuits	8-Bit	16-Bit
1.	CKD	$1.1179*10^{-04}$	$1.2110*10^{-04}$
2.	HSD	$1.1521*10^{-03}$	$1.4036*10^{-04}$
3.	LCR	$5.5290*10^{-09}$	$6.0532*10^{-09}$
4.	CKCCD	$3.7310*10^{-04}$	$3.7400*10^{-04}$
5.	SFLD	$1.1231*10^{-04}$	$1.1933*10^{-04}$
6.	DFD	$2.0310*10^{-03}$	$2.1035*10^{-03}$
7.	DPD	$2.3449*10^{-03}$	$2.4008*10^{-03}$
8.	CCD	$2.1601*10^{-10}$	$2.1708*10^{-10}$

C. Static Power Calculation

The static power components become important when the circuits are at rest, i.e. when there is no activity in the circuits and they are all biased to a specific state. Table. 2. Shows that the static power dissipation occurs in the different domino circuits for 8-bit and 16-bit.

TABLE 2. STATIC POWER CALCULATION

S.No	Domino circuits	8-Bit	16-Bit
1.	CKD	$2.0939*10^{-04}$	$2.1034*10^{-04}$
2.	HSD	$4.952*10^{-03}$	$5.0112*10^{-03}$
3.	LCR	$1.1001*10^{-03}$	$1.1291*10^{-03}$
4.	CKCCD	$1.5460*10^{-05}$	$1.6543*10^{-05}$
5.	SFLD	$1.9431*10^{-04}$	$2.890*10^{-04}$
6.	DFD	$8.3479*10^{-04}$	$8.3580*10^{-04}$
7.	DPD	$8.5237*10^{-04}$	$8.6011*10^{-04}$
8.	CCD	$1.5900*10^{-03}$	$1.6002*10^{-03}$

D .Dynamic Power Calculation

The power is consumed by a device when it is actively switching from one state to another. Dynamic power consists of switching power, consumed while charging and discharging the loads on a device, and internal power, consumed internal to the device while it is changing state. The Table 3 shows that the dynamic power dissipation occurs in the different domino circuits.

TABLE 3. DYNAMIC POWER CALCULATION

S.No	Domino circuits	8-Bit	16-Bit
1.	CKD	$3.2923*10^{-03}$	$3.3015*10^{-03}$
2.	HSD	$3.2895*10^{-03}$	$3.2902*10^{-03}$
3.	LCR	$4.0914*10^{-03}$	$4.1021*10^{-03}$
4.	CKCCD	$1.57921*10^{-04}$	$1.5943*10^{-04}$
5.	SFLD	$2.1093*10^{-03}$	$2.1873*10^{-03}$
6.	DFD	$7.6464*10^{-04}$	$7.6507*10^{-04}$
7.	DPD	$5.0016*10^{-04}$	$5.0021*10^{-04}$
8.	CCD	$1.0713*10^{-04}$	$1.0734*10^{-04}$

E. Delay Calculation

The delay is defined as the average of rise time and fall time between the input and output. The delay occurs in the various domino circuits and its decrease the speed of the circuit. The Table 4 shows that delay occurs in the different domino circuits for 8-bit and 16-bit.

TABLE 4. DELAY CALCULATION

S.No	Domino circuits	8-Bit	16-Bit
1.	CKD	$5.138*10^{-13}$	$2.187*10^{-12}$
2.	HSD	$7.44*10^{-13}$	$2.44*10^{-12}$
3.	LCR	$1.202*10^{-12}$	$3.980*10^{-12}$
4.	CKCCD	$1.938*10^{-12}$	$2.00*10^{-12}$
5.	SFLD	$1.725*10^{-12}$	$1.352*10^{-12}$
6.	DFD	$2.561*10^{-12}$	$2.568*10^{-12}$
7.	DPD	$4.394*10^{-12}$	$4.361*10^{-12}$
8.	CCD	$3.894*10^{-13}$	$4.088*10^{-13}$

VI. CONCLUSION

In this paper, the delay, leakage, static and dynamic power dissipation with various domino circuits such as conditional keeper domino, high speed domino, leakage current replica keeper, controlled keeper by current comparison domino, standard footless domino, diode footed domino, diode partitioned domino, wide OR gate current comparison based domino circuits are compared with 8-bit and 16-bit using CADENCE 180nm technology. It is observed that the leakage power and delay are reduced in wide OR gate using current comparison based domino circuits (CCD).

VII. FUTURE SCOPES

In future work, various domino circuits are compared with 8-bit, 16-bit, and 32-bit and 64 bit based on the variable threshold CMOS (VTCMOS) technique and it is designed using GPDK 90nm technology. The future work is to achieve better performance with reduced leakage power, delay and noise immunity.

REFERENCES

[1] L. Wang, R. Krishnamurthy, K. Soumyanath, and N. Shanbhag, "An energy-efficient leakage-tolerant dynamic circuit technique," in *Proc. Int. ASIC/SoC Conf.*, 2000, pp. 221–225.

[2] A. Alvandpour, R. Krishnamurthy, K. Sourrty, and S. Y. Borkar, "A sub-130-nm conditional-keeper technique," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 633–638, May 2002.

[3] M. H. Anis, M. W. Allam, and M. I. Elmasry, "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 10, no. 2, pp. 71–78, Apr. 2002.

[4] Y. Lih, N. Tzartzanis, and W. W. Walker, "A leakage current replica keeper for dynamic circuits," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 48–55, Jan. 2007.

[5] A. Peiravi and M. Asyaei, "Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates, integration," *VLSI J.*, vol. 45, no. 1, pp. 22–32, 2012.

[6] H. Mahmoodi and K. Roy, "Diode-footed domino: A leakage-tolerant high fan-in dynamic circuit design style," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 3, pp. 495–503, Mar. 2004.

[7] H. Suzuki, C. H. Kim, and K. Roy, "Fast tag comparator using diode partitioned domino for 64-bit microprocessors," *IEEE Trans. Circuits Syst.*, vol. 54, no. 2, pp. 322–328, Feb. 2007.

[8] Ali Peiravi and Mohammad Asyaei," Current-Comparison-Based Domino: New Low-Leakage High-Speed Domino Circuit for Wide Fan-In Gates," *IEEE Trans on very large scale integration systems*, vol. 21, no. 5, May 2013.